
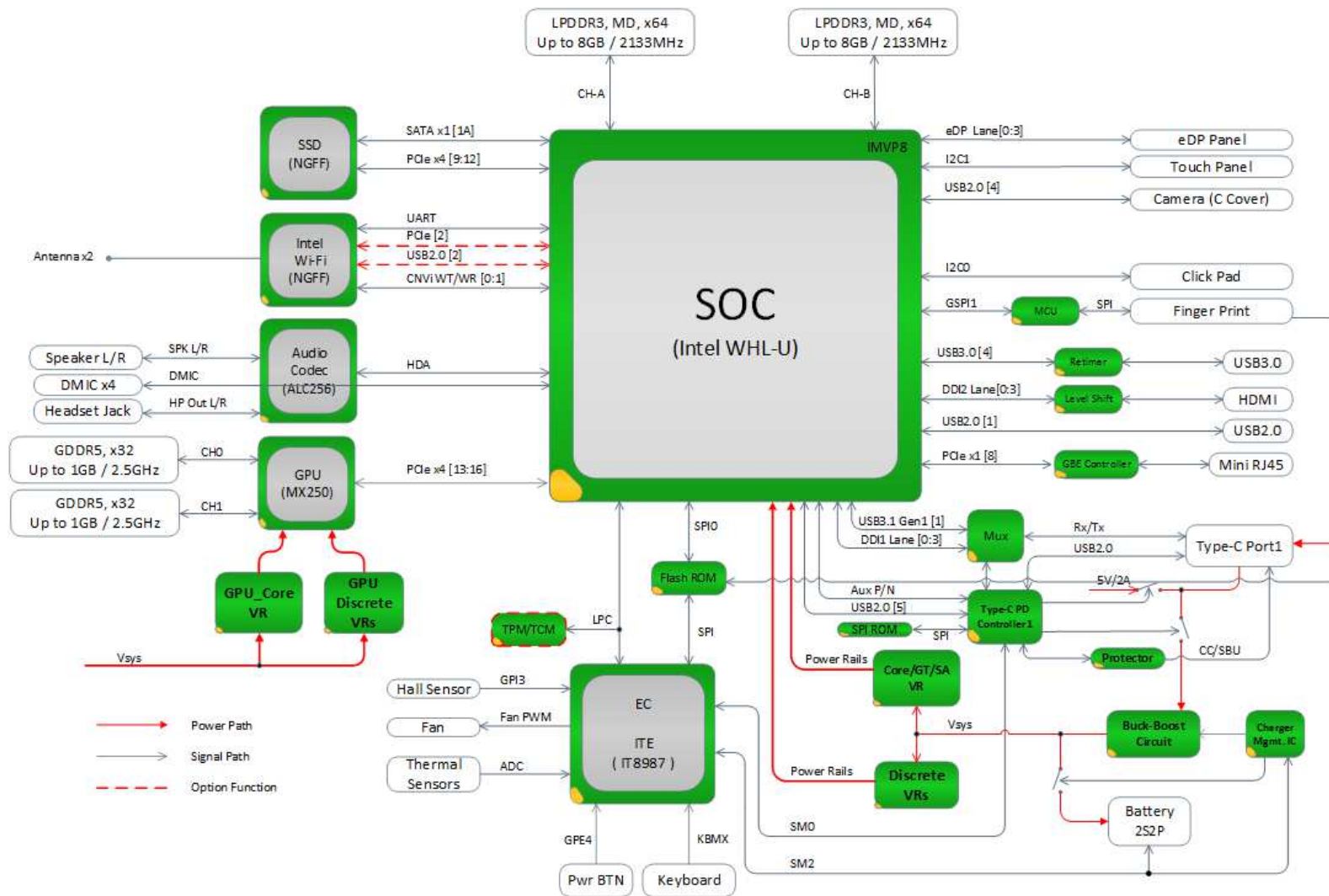



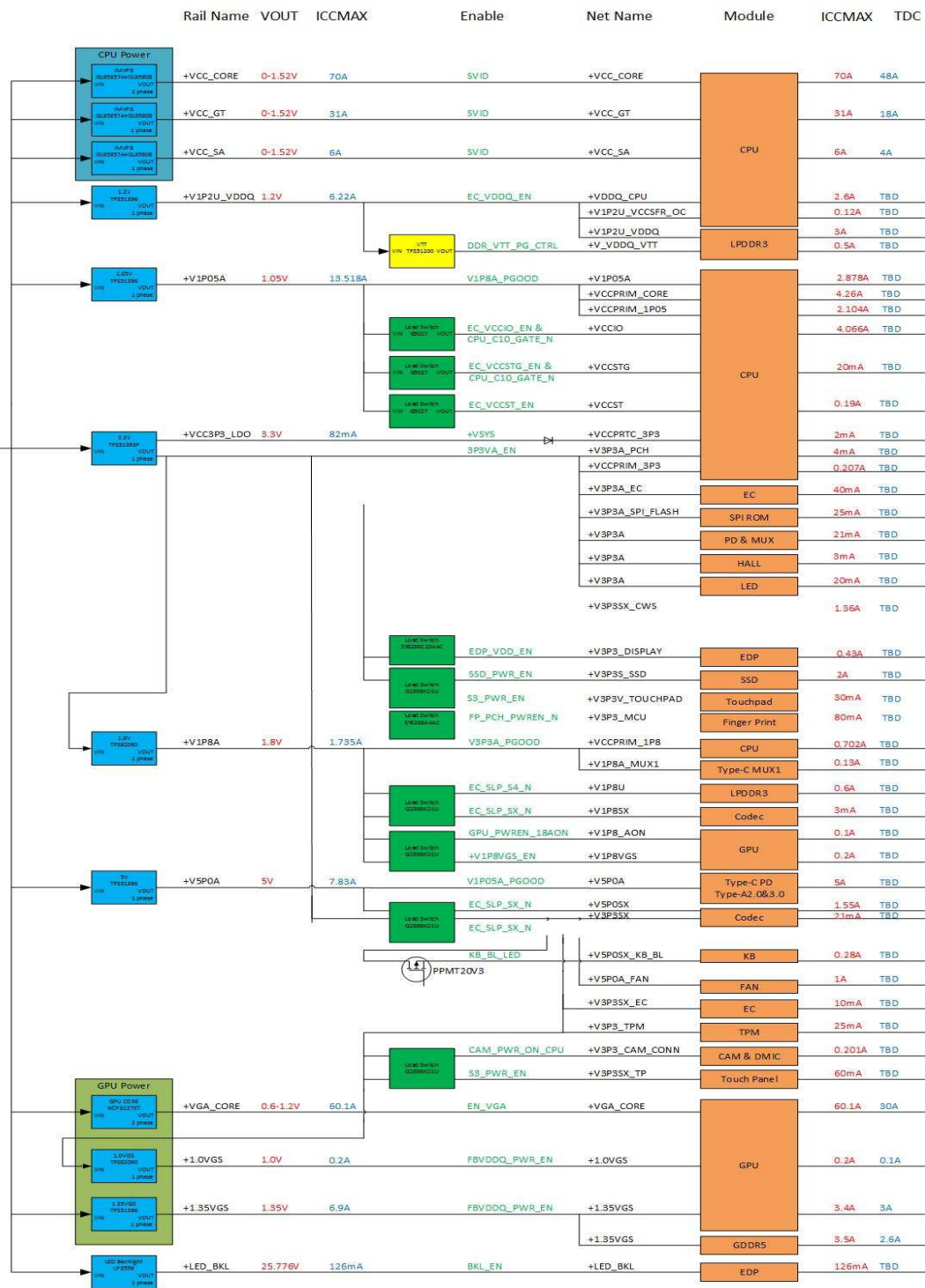
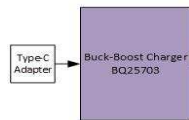
Schematics Page Index (Title / Revision / Change Date)

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08	WHL-U42 (DISPLAY)	1.0		42	EC (IT8987E)	1.0	
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12	WHL-U42 (USB/PCIE)	1.0		46	RSMRST OFF	1.0	
13	WHL-U42 (PMU)	1.0		47	N17S PCIE/ CLK/ GPIO	1.0	
14	WHL-U42 (VCORE/GT)	1.0		48	N17S DISPLAY/ STRAP/ JTAG	1.0	
15	WHL-U42 (PCH)	1.0		49	N17S MEM Power	1.0	
16	WHL-U42 (VCC/VDDQ)	1.0		50	N17S +VGA CORE, GND	1.0	
17	WHL-U42 (VSS)	1.0		51	N17S MEM Interface	1.0	
18	WHL-U42 (CFG)	1.0		52	N17S GDDR5	1.0	
19	WHL-U42 (DECOUPLING1)	1.0		53	N17S MISC	1.0	
20	WHL-U42 (DECOUPLING2)	1.0		54	sensor	1.0	
21	WHL-U42 (DECOUPLING3)	1.0		55	TPM	1.0	
22	WHL-U42 (DECOUPLING4)	1.0		56	POWER DCIN & BATTERY CHARGER	1.0	
23	LPDDR3 CH-A 1	1.0		57	POWER DELIVERY 3.3V	1.0	
24	LPDDR3 CH-A 2	1.0		58	POWER DELIVERY 5V	1.0	
25	LPDDR3 CH-B 1	1.0		59	POWER DELIVERY 1.8V	1.0	
26	LPDDR3 CH-B 2	1.0		60	POWER DELIVERY 1.05V	1.0	
27	LPDDR3 (DECAPS)	1.0		61	POWER DELIVERY-IMVP1	1.0	
28	LPDDR3 TERMINATIONS	1.0		62	POWER DELIVERY 1.2V	1.0	
29	SYSTEM FLASH	1.0		63	POWER DELIVERY 1.35VGS	1.0	
30	TYPE1-C CONN	1.0		64	POWER DELIVERY 1.0VGS&1.8VGS	1.0	
31	TYPE1-C PD & MUX	1.0		65	POWER DELIVERY-GPU Core	1.0	
32	USB3.0&2.0	1.0		66	POWER DELIVERY Load switch	1.0	
33	LAN	1.0		67	LED BACKLIGHT	1.0	
34	BLANK	1.0		68	Debug Conn	1.0	
				69	Hole & Mark	1.0	
				70	Changelist	1.0	

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Page name: Index		
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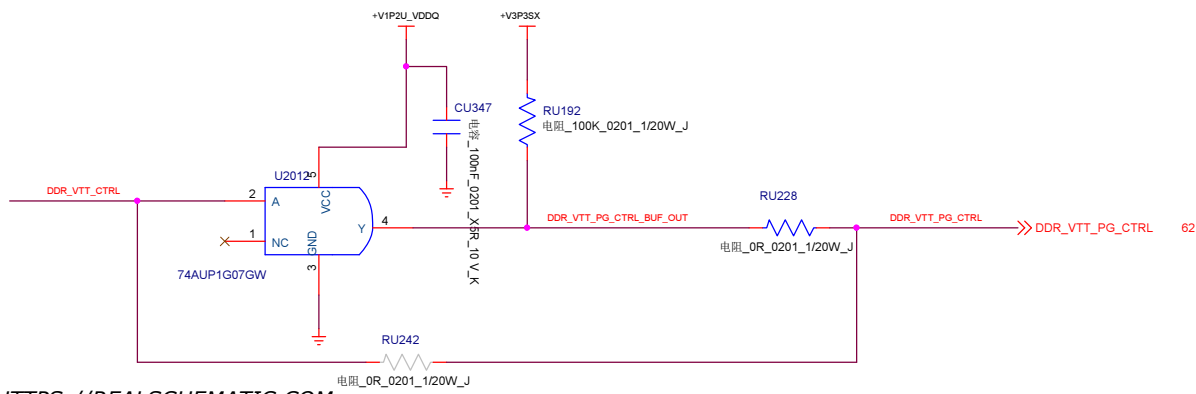


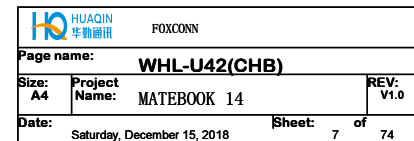
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Page name: Block Diagram			
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I2C Allocation Mapping

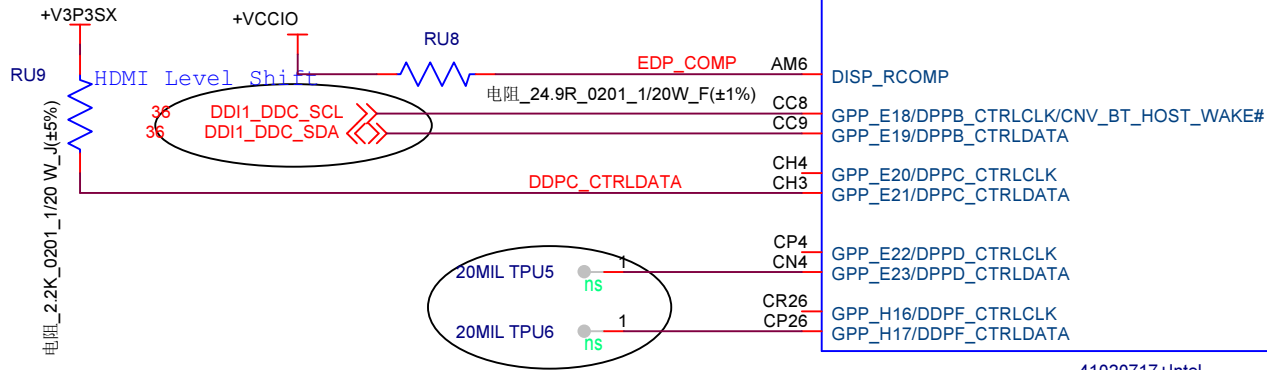
EC	Device1		Device2			Device3
SMCLK0	Type-C1(PD)	0x40	x	x	x	x
SMDAT0						
SMCLK1	Battery	0x16	x	x	x	x
SMDAT1						
SMCLK2	Charger	0xD6	GPU	0x9E	LCD Back Light	0x58
SMDAT2						
SMCLK3	Debug	address:TBD	x	x	x	x
SMDAT3						
SOC	Device1		Device2		Device3	
I2C_CLK0	TOUCHPAD	0x15	X	X	X	X
I2C_DAT0						
I2C_CLK1	TOUCHPAENL	0x10	X	X	X	X
I2C_DAT1						
I2C_CLK2	X	X	X	X	X	X
I2C_DAT2						
I2C_CLK3	X	X	X	X	X	X
I2C_DAT3						
I2C_CLK4	X	X	X	X	X	X
I2C_DAT4						
I2C_CLK4B	X	X	X	X	X	X
I2C_DAT4B						
ISH_I2C_CLK0	X	X	X	X	X	X
ISH_I2C_DAT0						
ISH_I2C_CLK1	X	X	X	X	X	X
ISH_I2C_DAT1						
ISH_I2C_CLK2	X	X	X	X	X	X
ISH_I2C_DAT2						





HDMI DDI


TypeC DP DDI

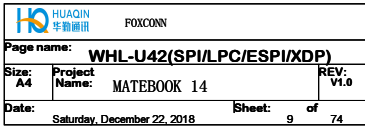


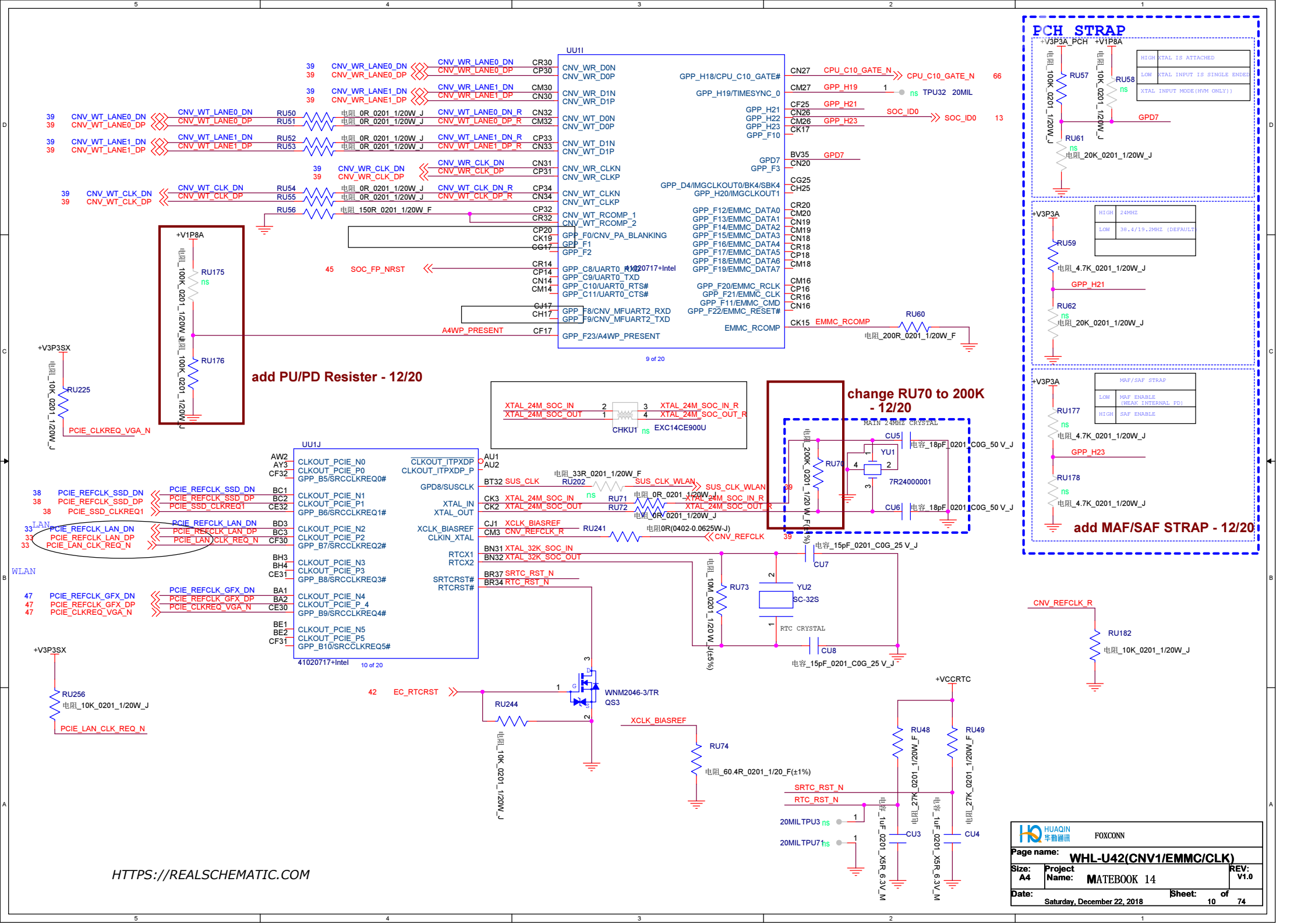
DISPLAY PORT STRAP

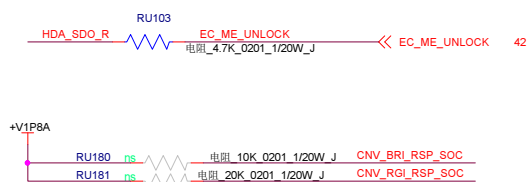
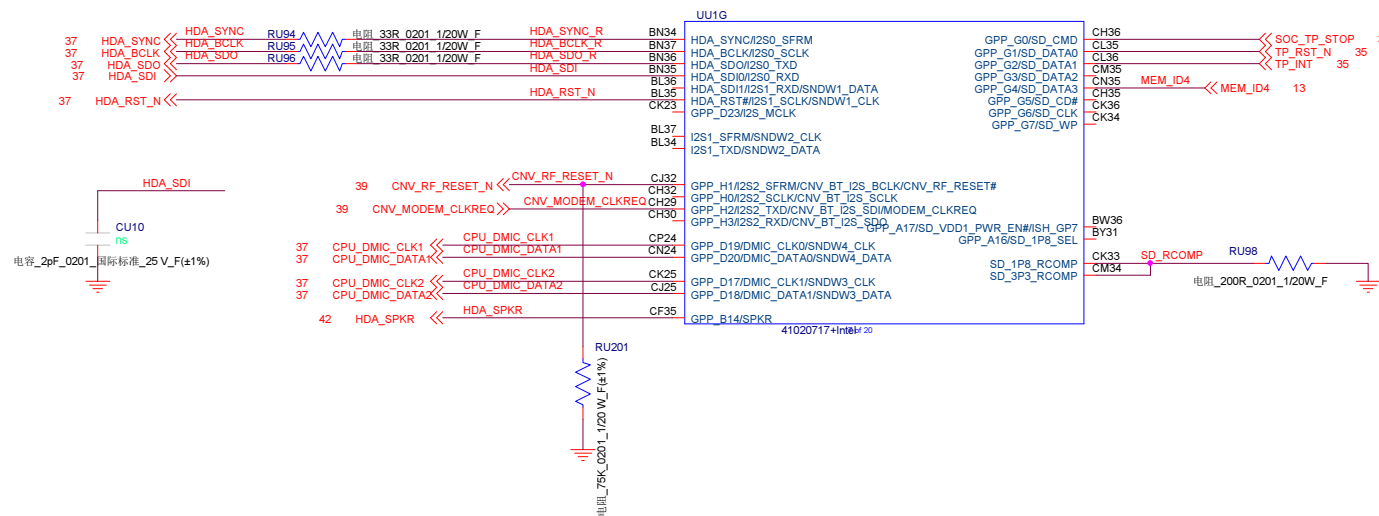
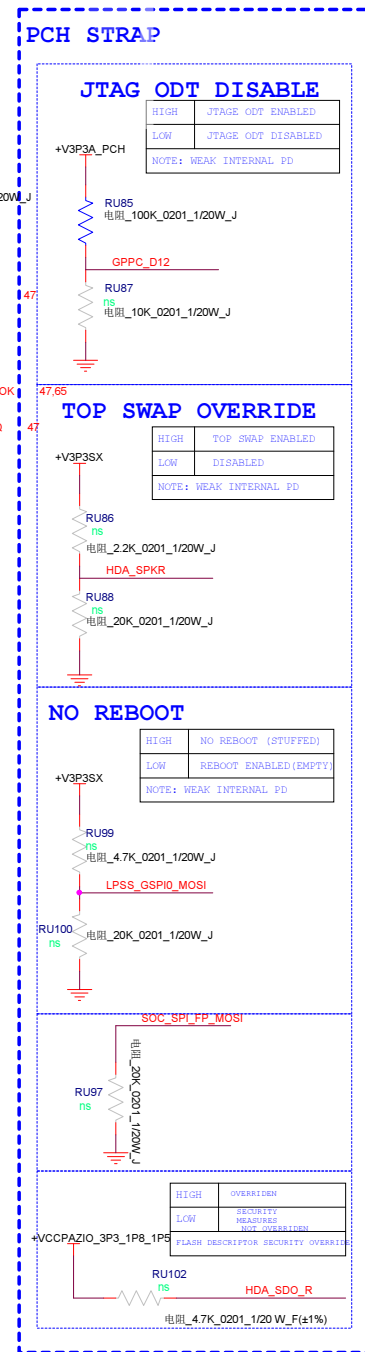
Strap	How to Enable Port	How to Disable Port	Matched HPD	DISP_RCOMP
DDI Port 1 DDPB_CTRLDATA	Pull up to 3.3 V With 2.2K	No Connect (default)	DDPB_HPD0	DISPLAY (HDMI/eDP*/DisplayPort*) 24.9Ω ±1% to VCCIO
DDI Port 2 DDPC_CTRLDATA	Pull up to 3.3 V With 2.2K (default)	No Connect	DDPC_HPD1	
eDP Port NA	NA	NA	EDP_HPD	

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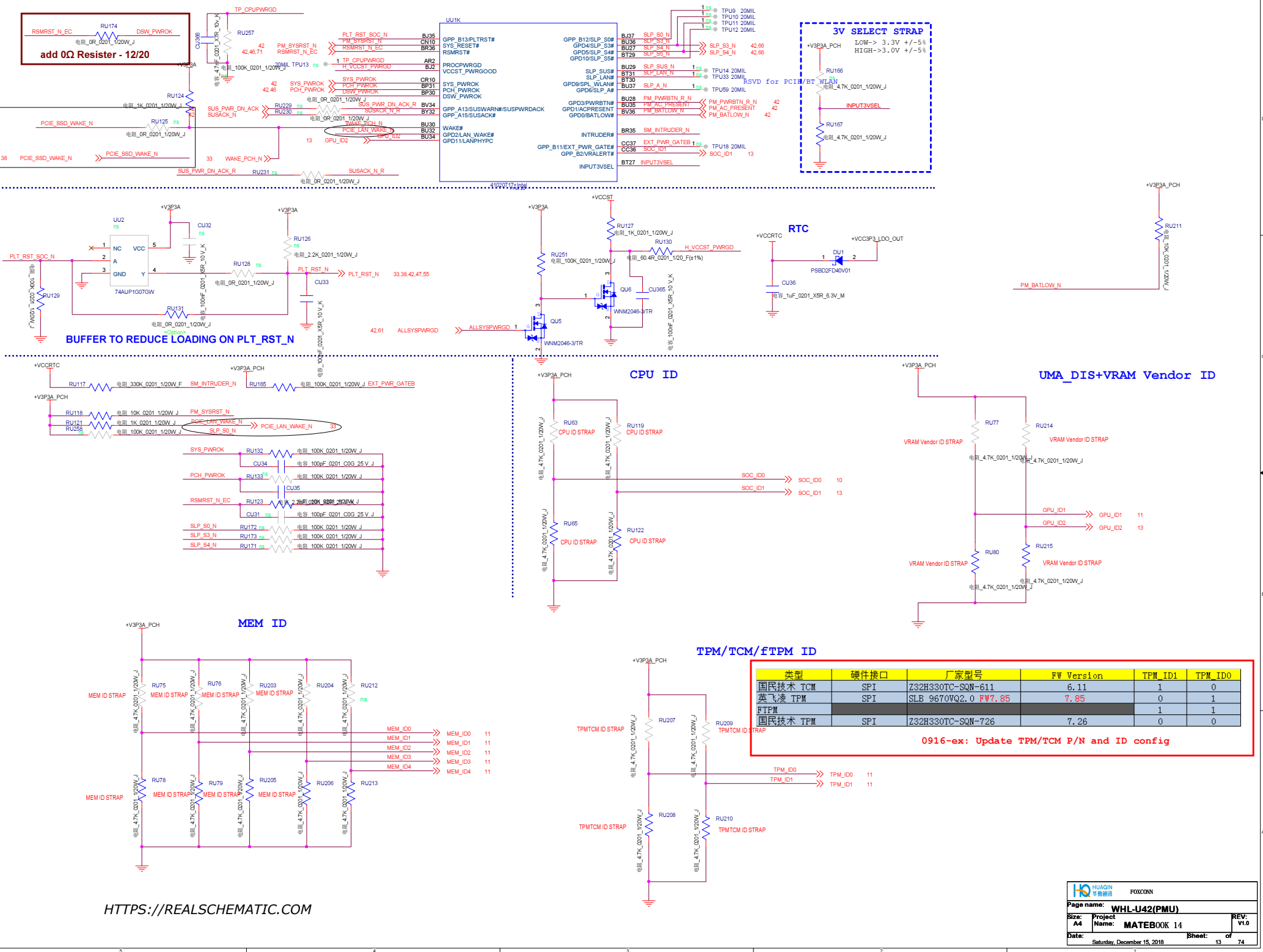
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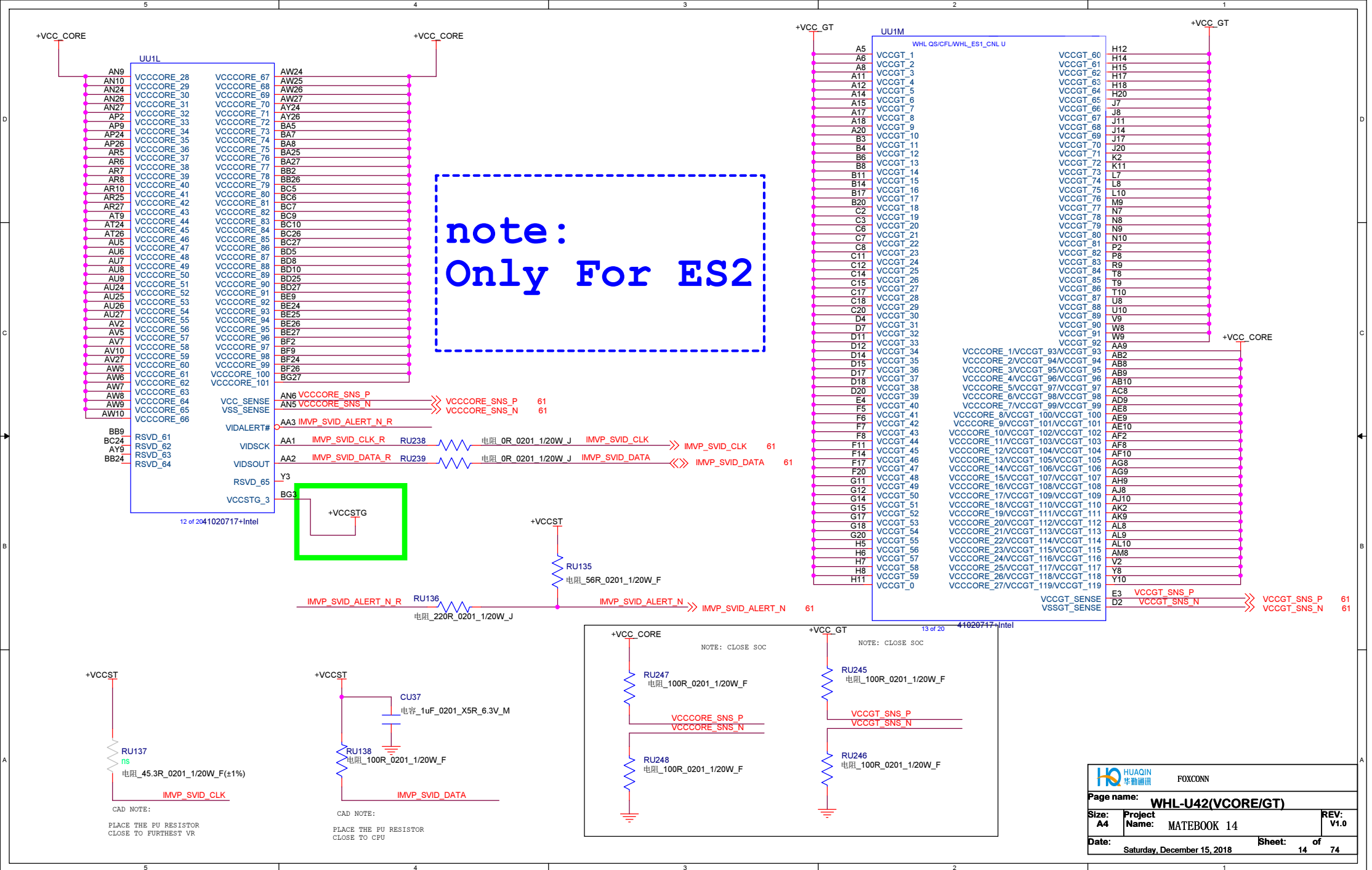


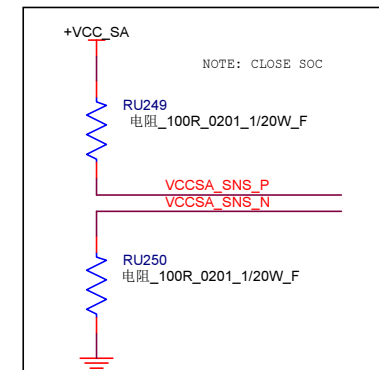
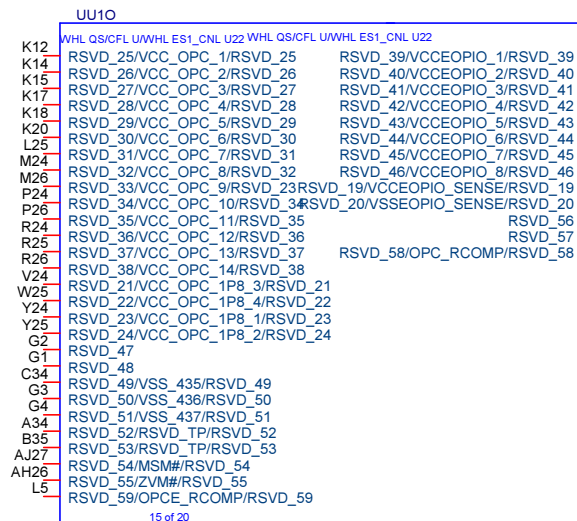
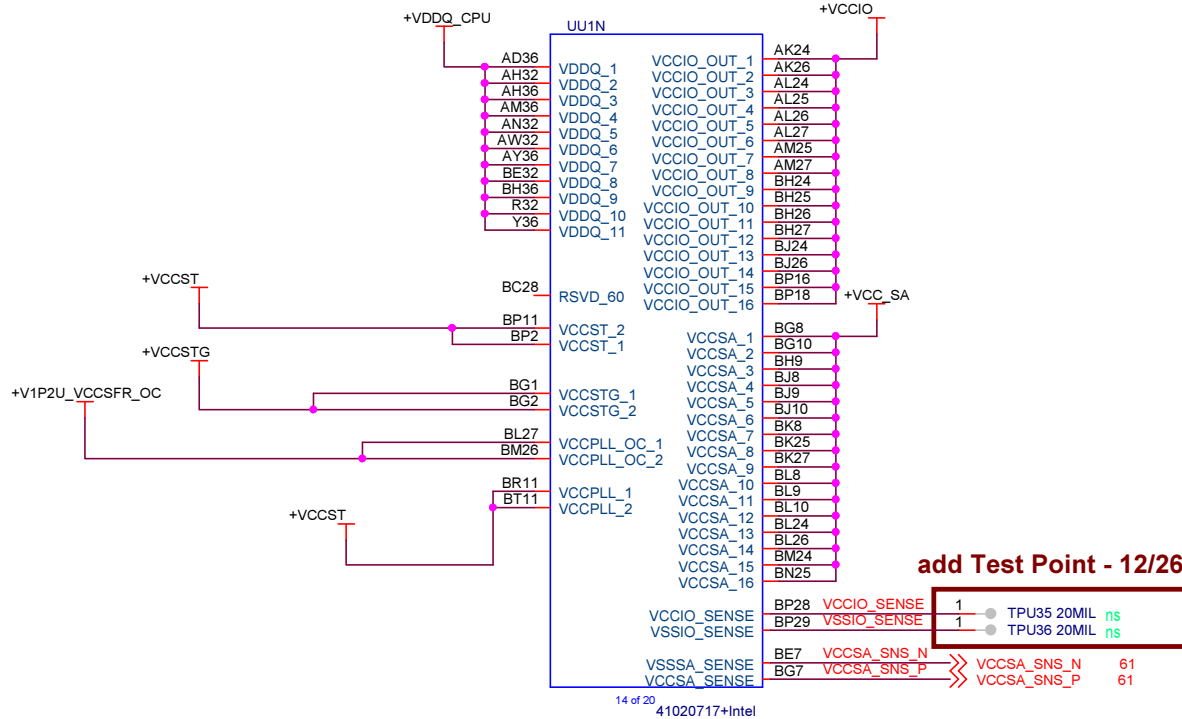
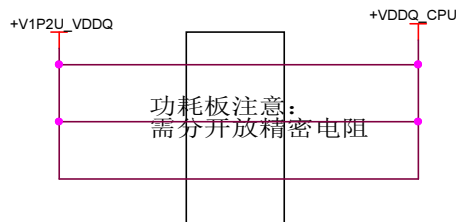


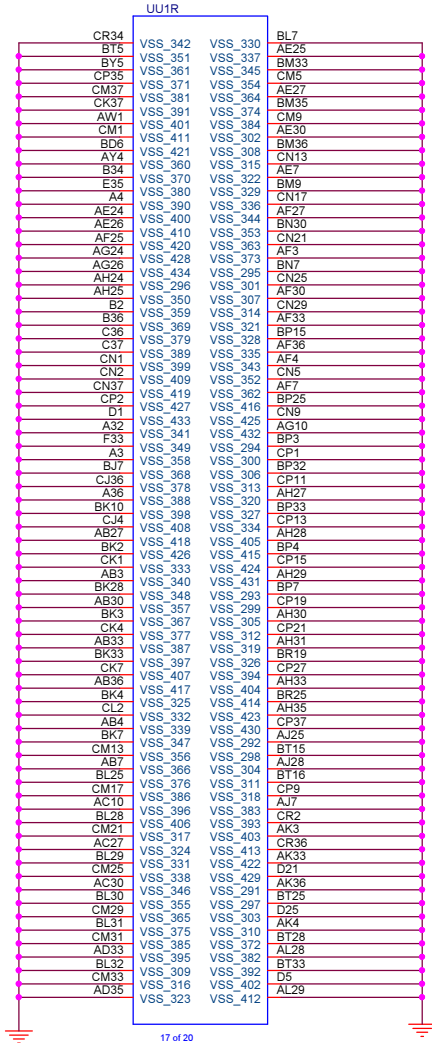
add 0Ω Resistor - 12/20



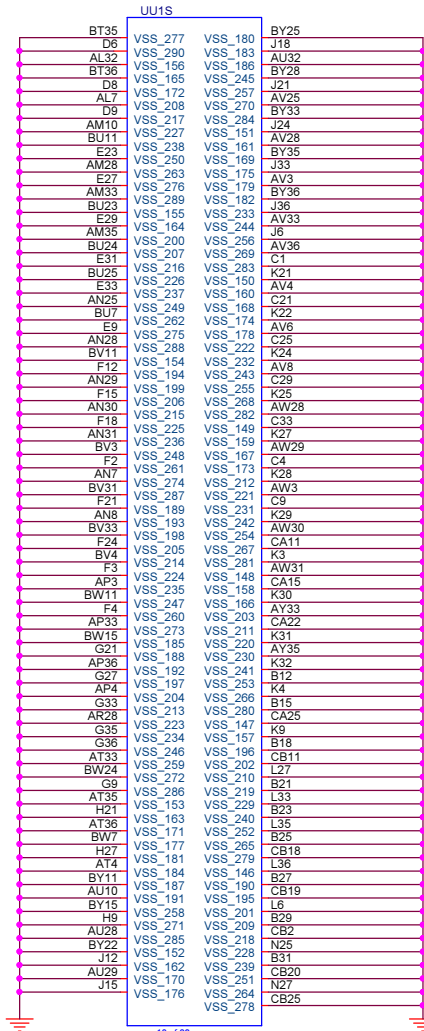
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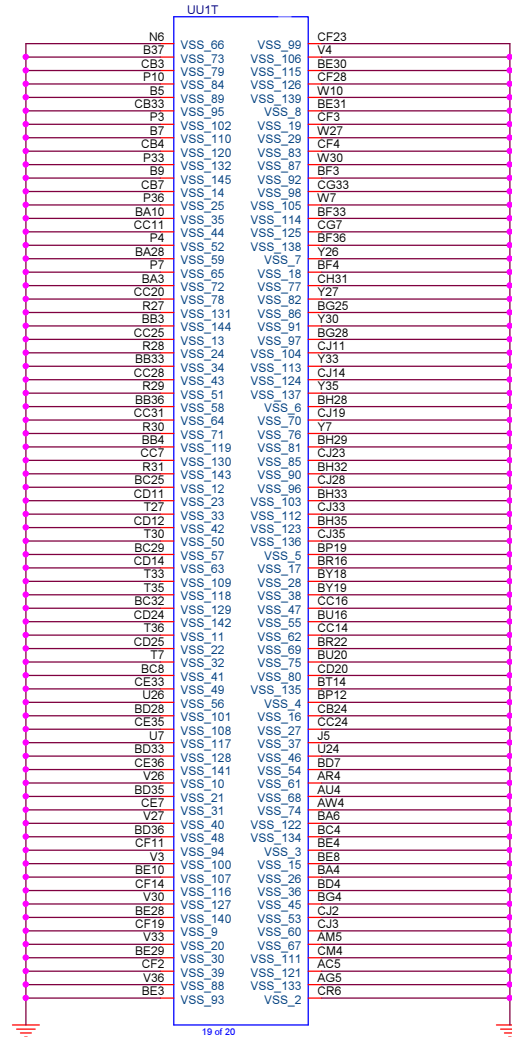




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41020717+Intel



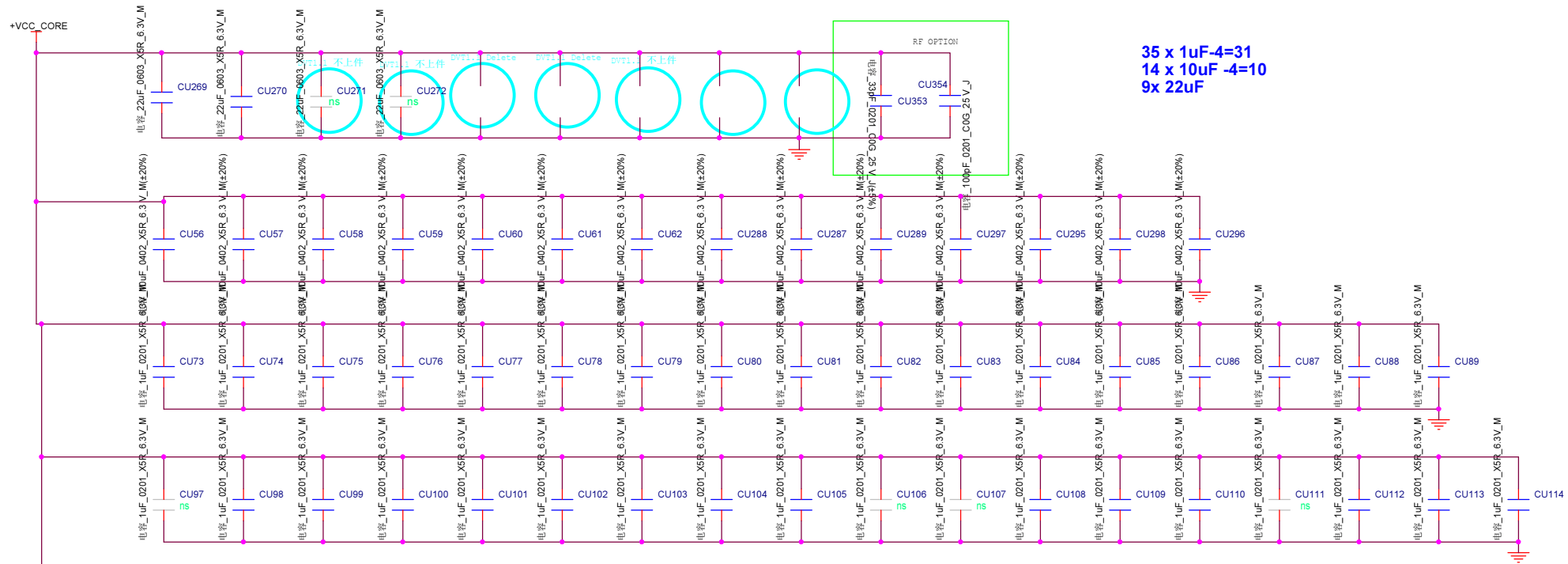
18 of 20
41020717+Intel



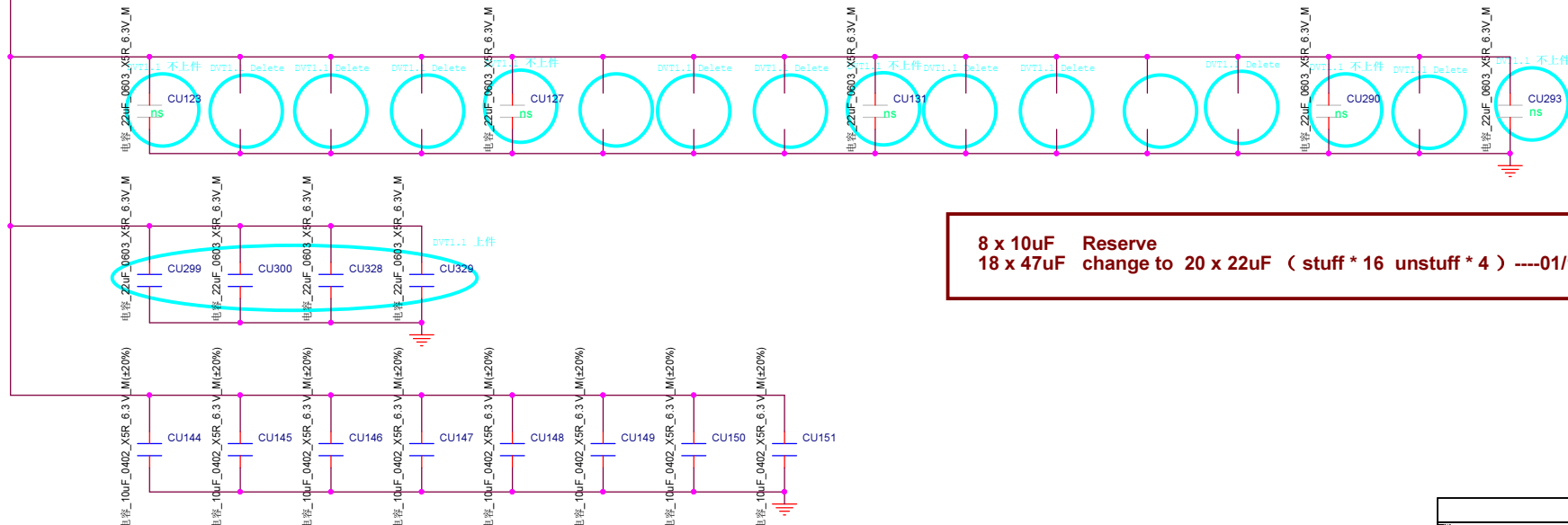
19 of 20
41020717+Intel

PLACE THESE CAPS UNDERNEATH BGA AREA

+VCCCORE



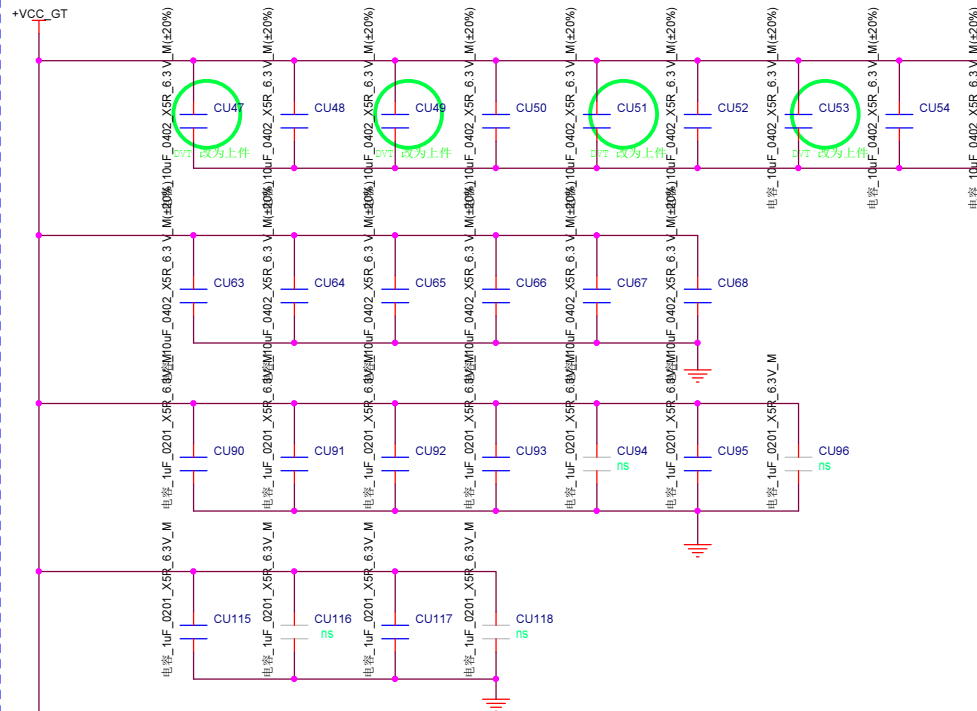
PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



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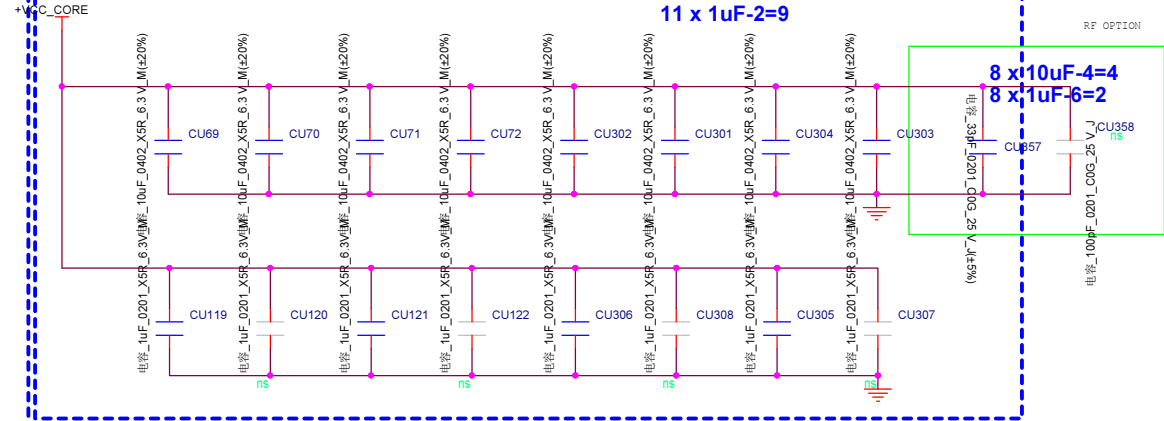
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+VCCGT

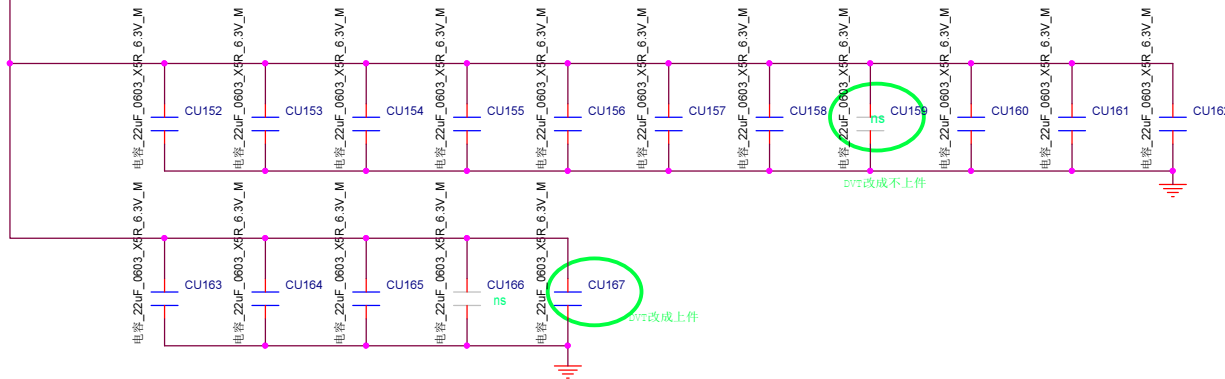
PLACE THESE CAPS UNDERNEATH BGA AREA

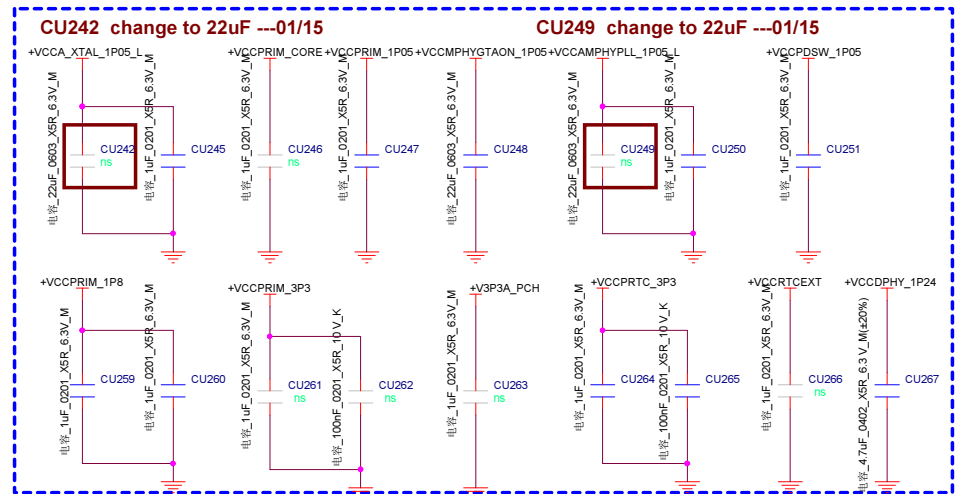
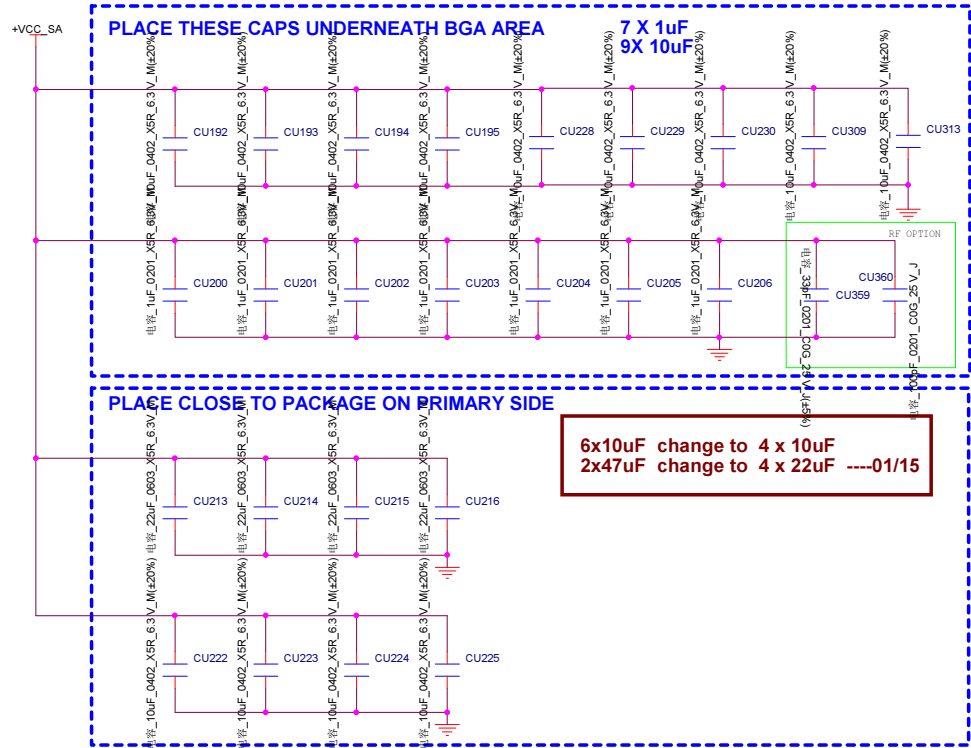
15 x 10uF
11 x 1uF-2=9

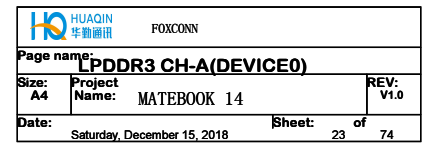


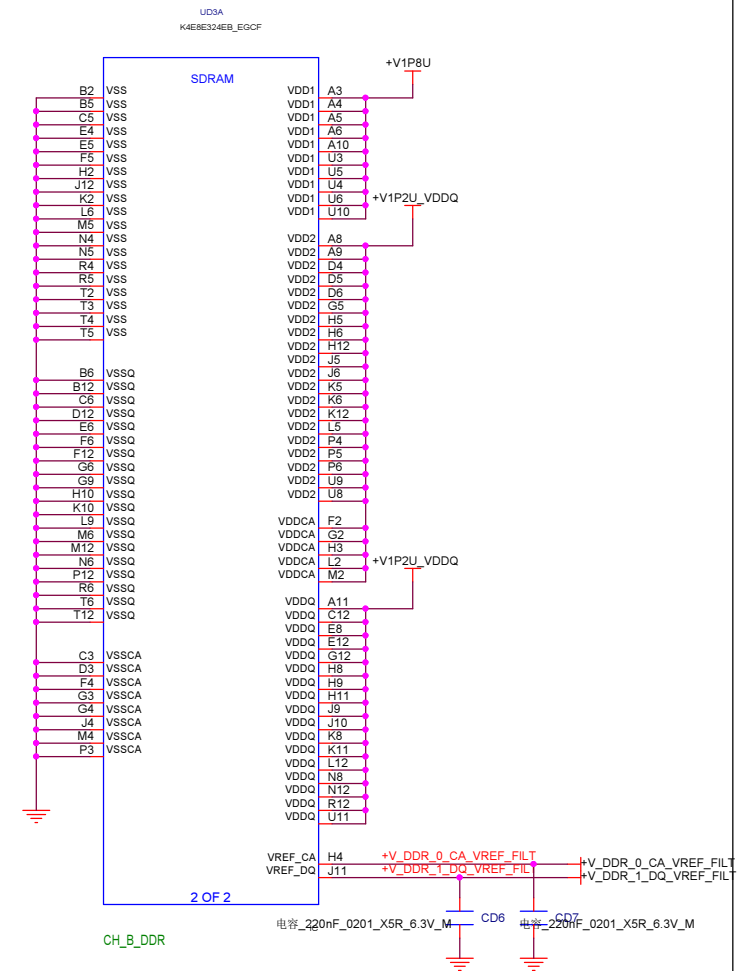
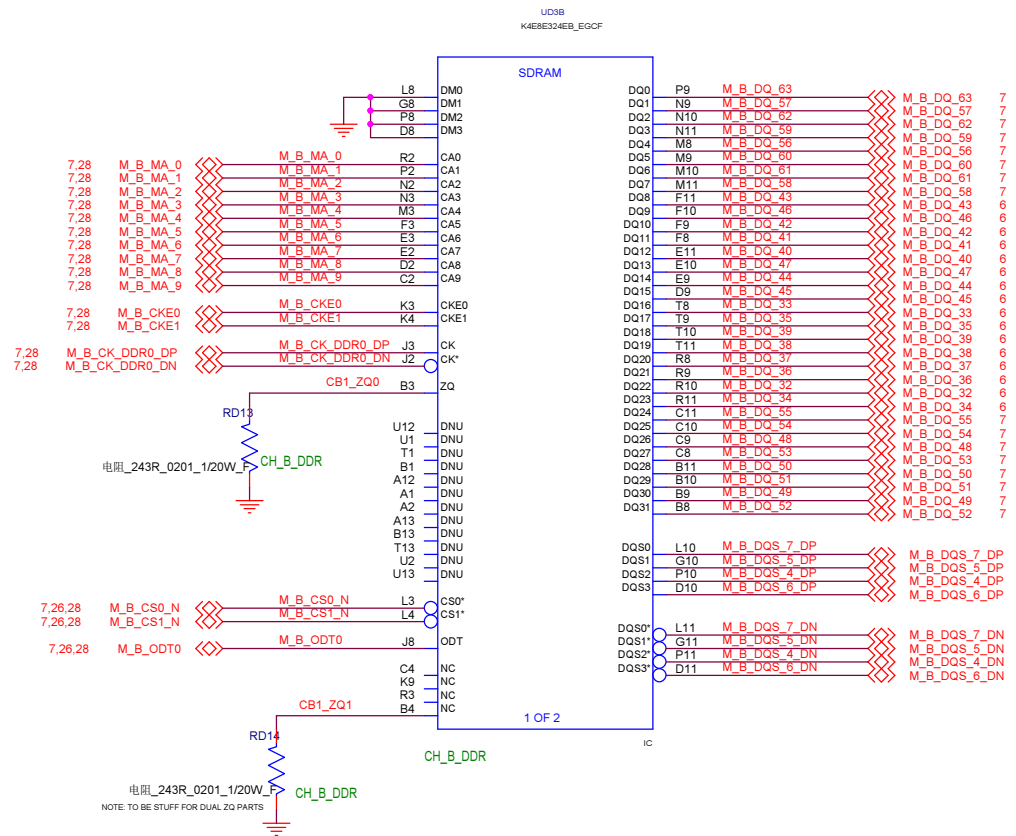
PLACE CLOSE TO PACKAGE ON PRIMARY SIDE

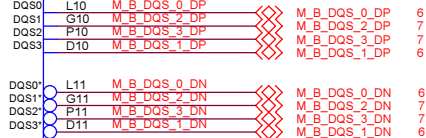
15 x 22uF change to 16 x 22uF (stuff * 14 unstuff * 2)
8 x 47uF delete ----01/15





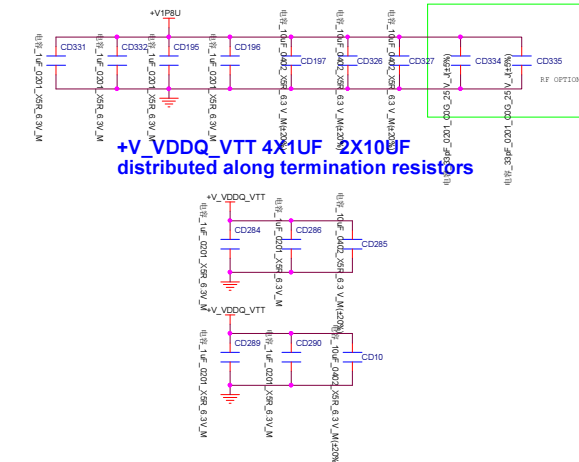
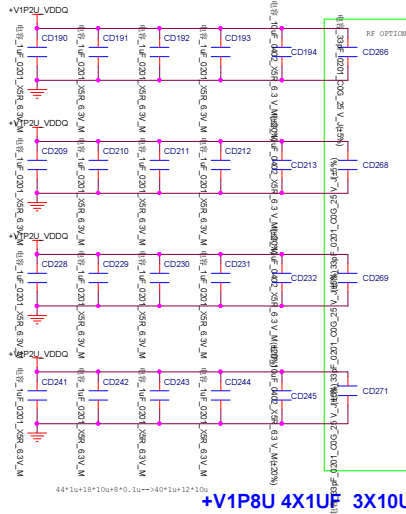






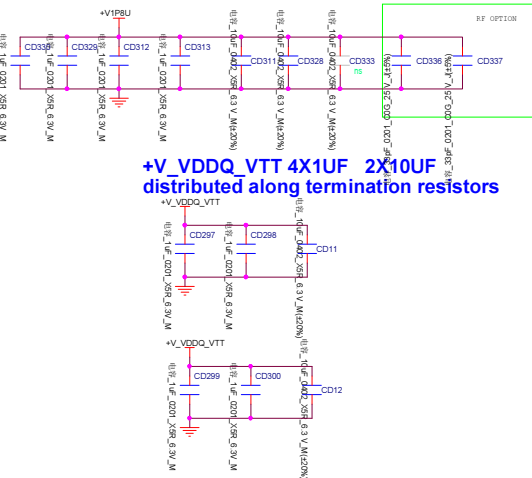
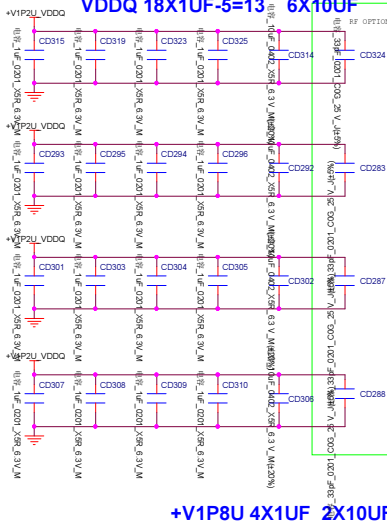
DECOUPLING CAPACITORS FOR DDR CHANNEL A

VDDQ 18X1UF-5=13 6X10UF+1=7

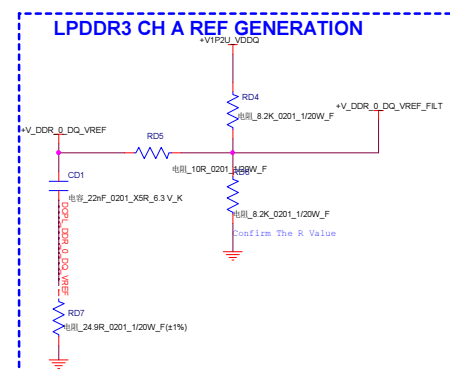
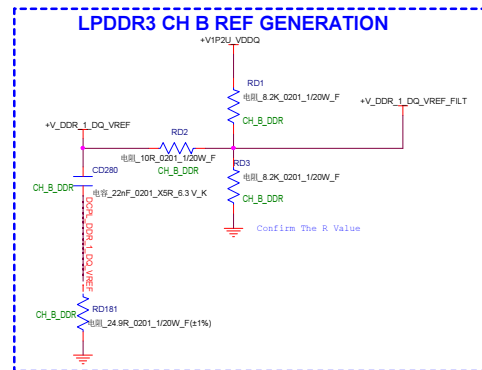
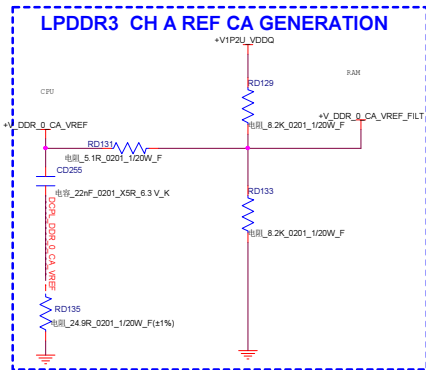


DECOUPLING CAPACITORS FOR DDR CHANNEL B

VDDQ 18X1UF-5=13 6X10UF



All caps need to put to DRAM as close as possible.



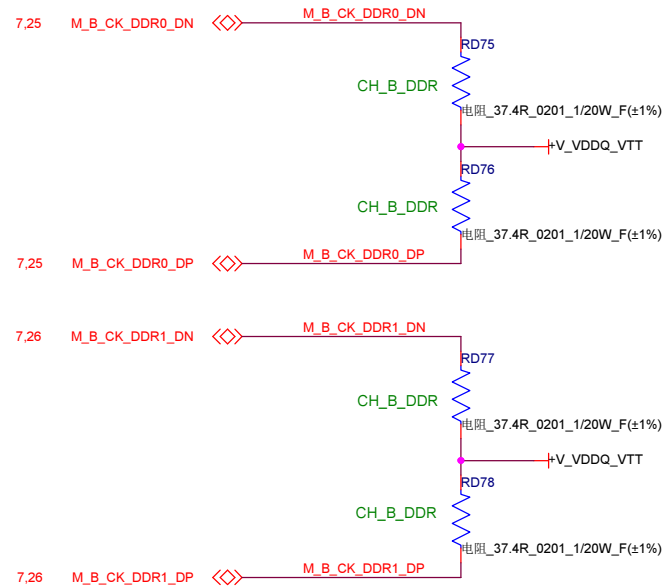
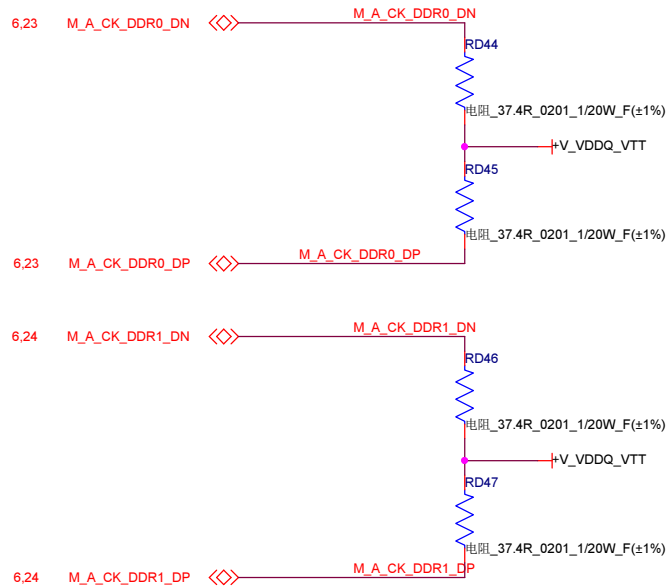
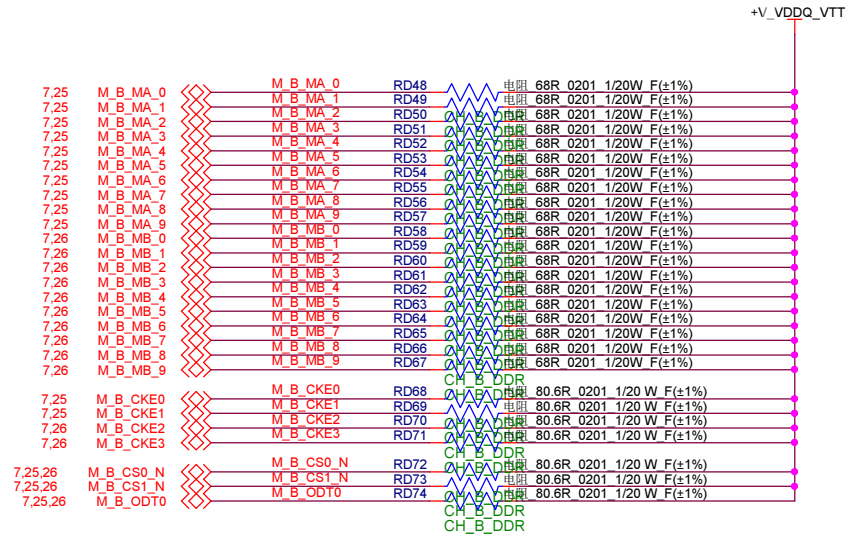
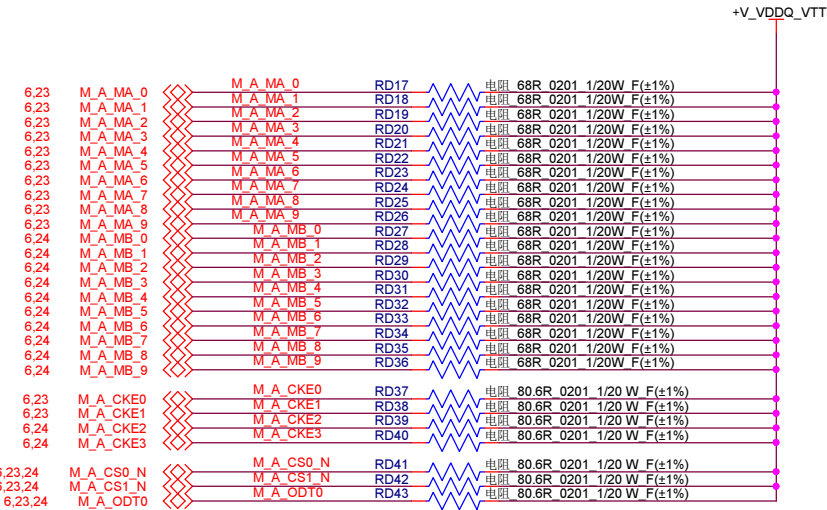
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MEMORY TERMINATIONS

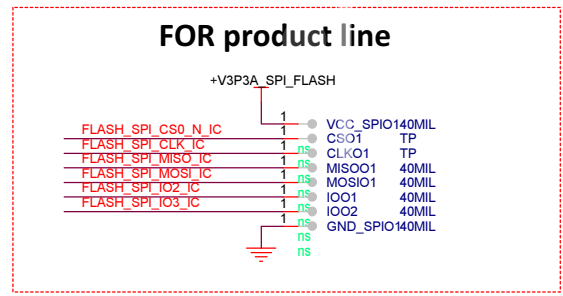
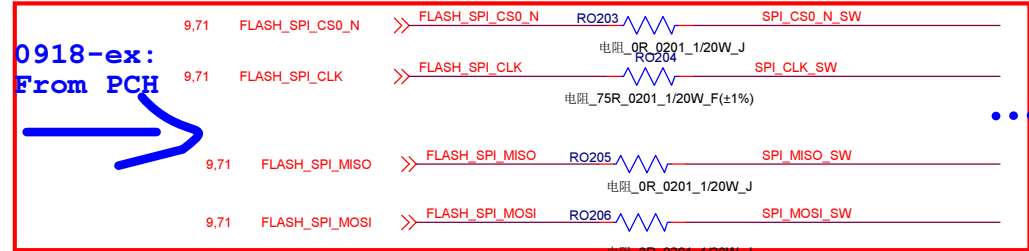
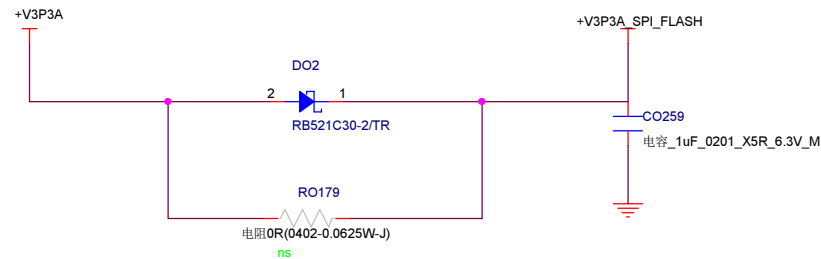
CHANNEL A

MEMORY TERMINATIONS

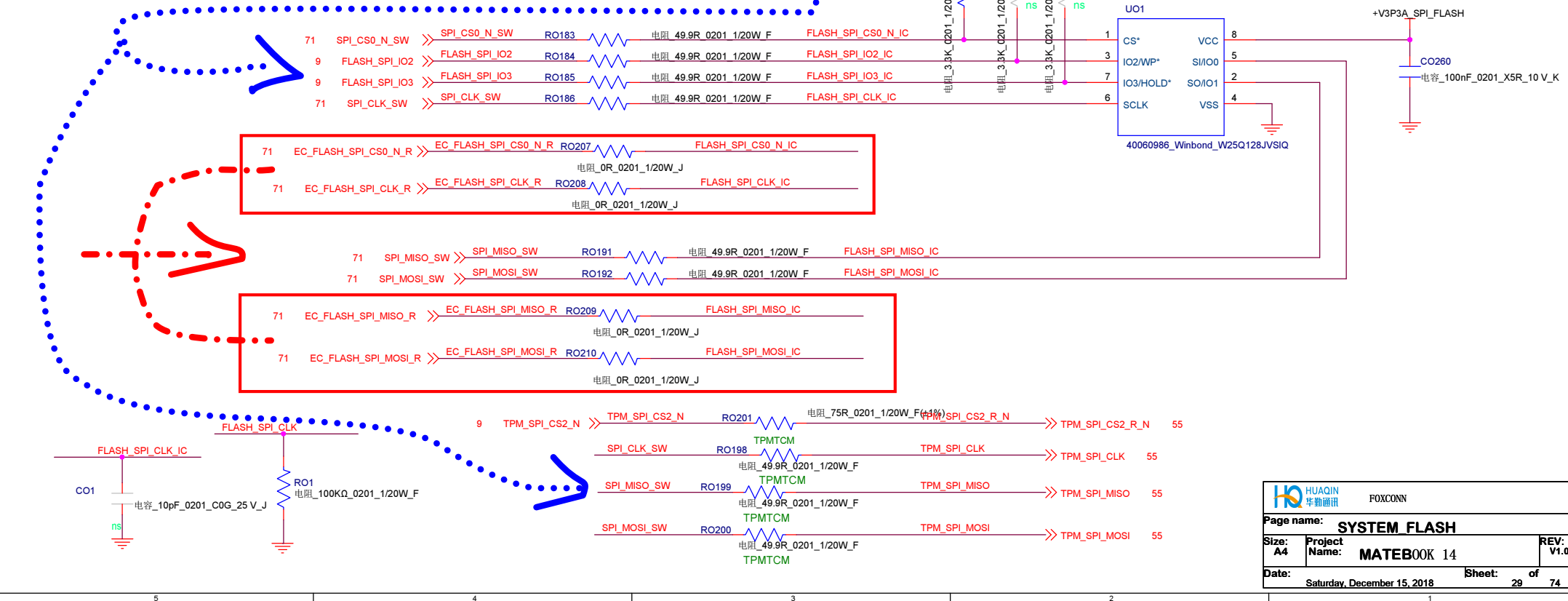
CHANNEL B




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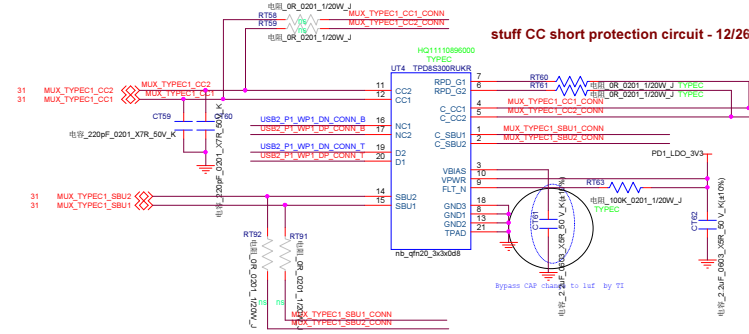
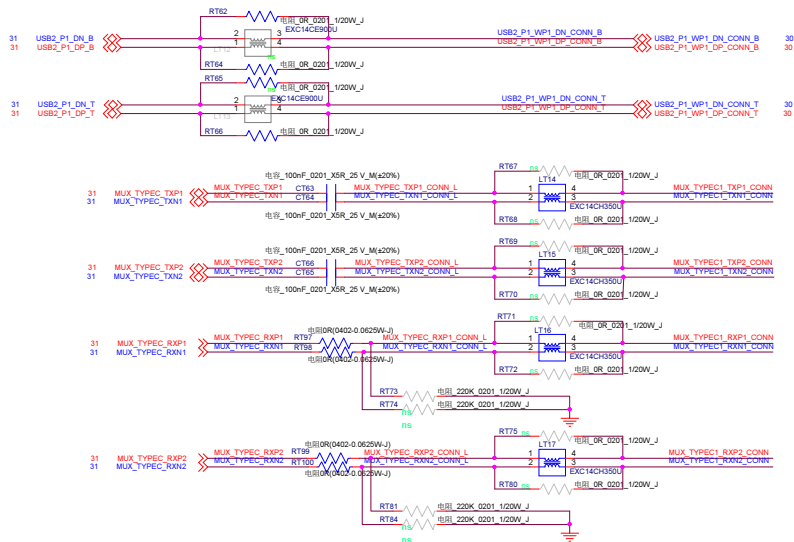


0916-ex:
by pass by 0 ohm resistors



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Page name: SYSTEM FLASH			
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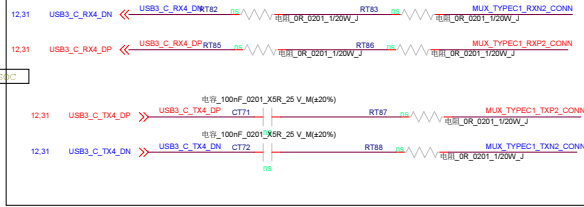
change the C (and R) and CMC
relative location



stuff CC short protection circuit - 12/26

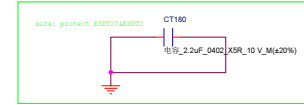
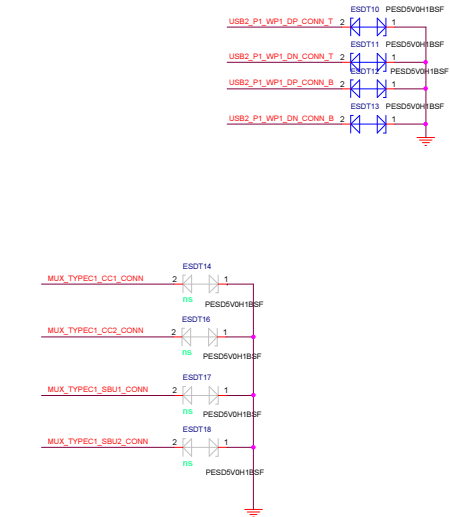
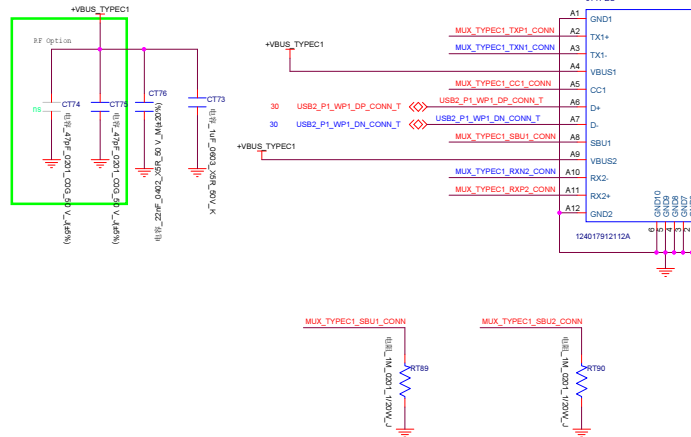
Bypass CAP channel to lnd by T1

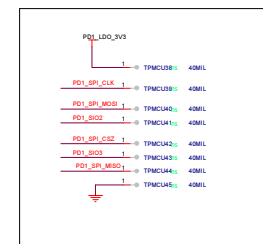
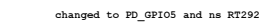
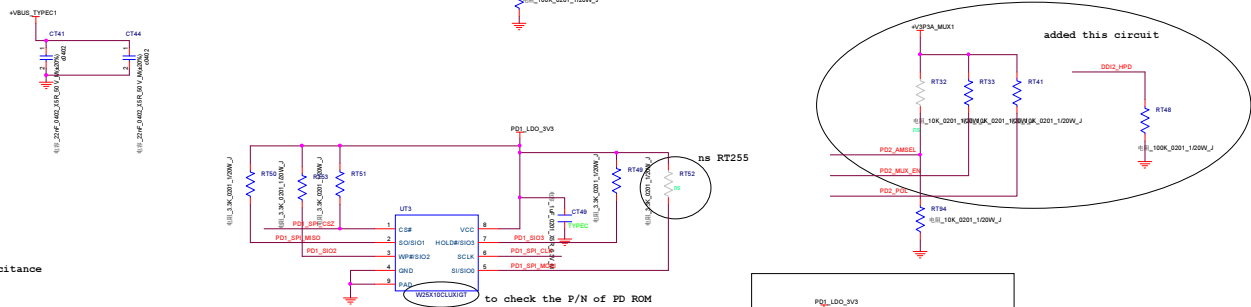
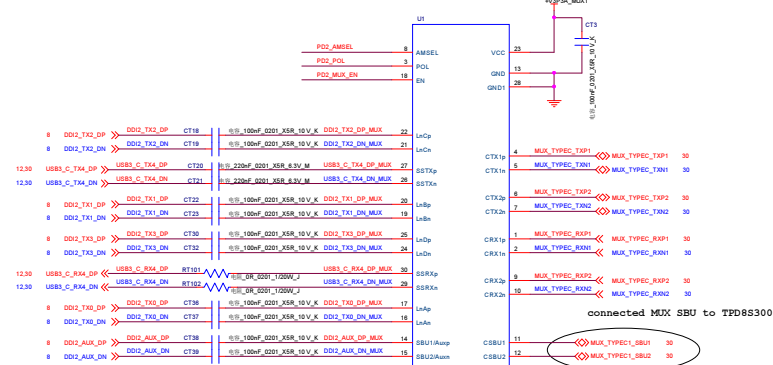
DCI Debug




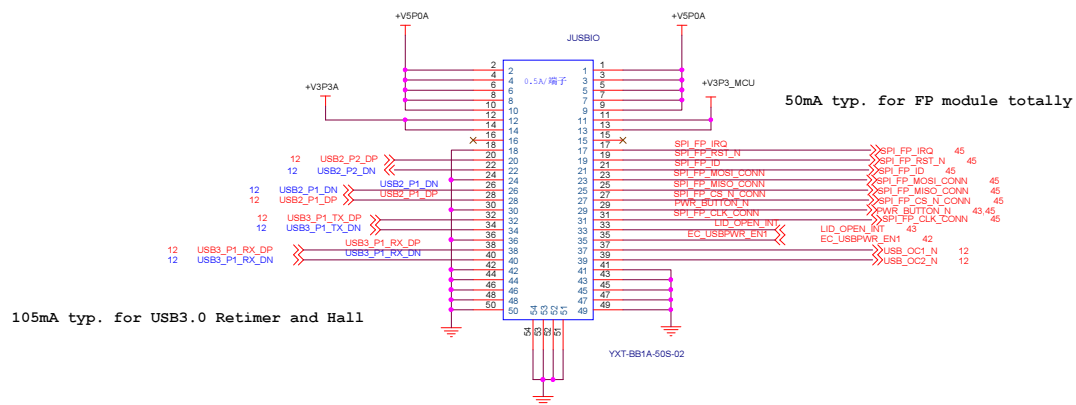
output to E9C

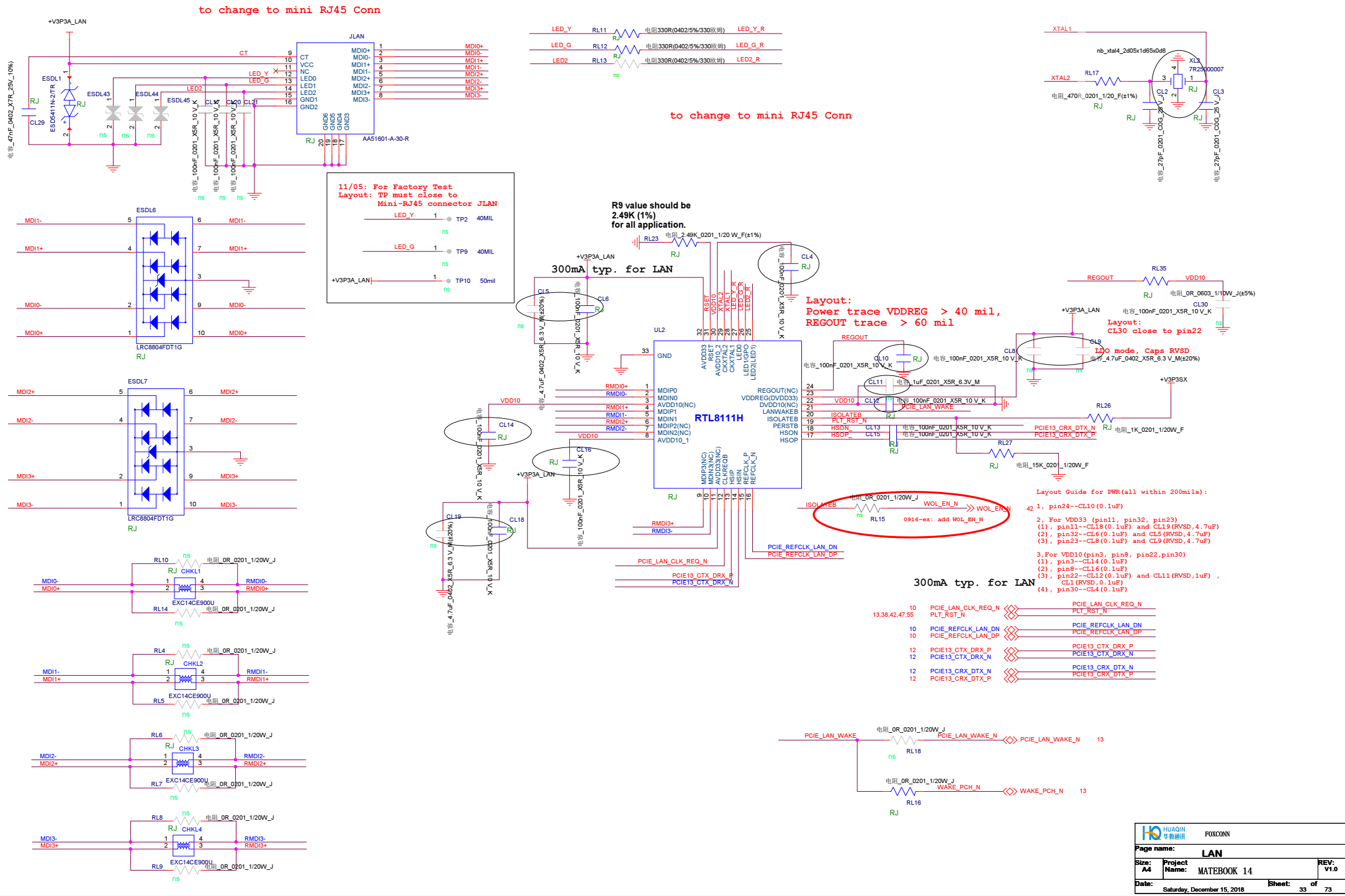
0606---与龙专确认 EMC 型号OK, 料号待确认OK






 HUADIN 华电国际		FUSCON	
Page name: TYPE-C PD & MUX			
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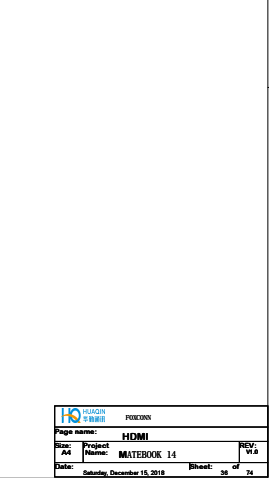
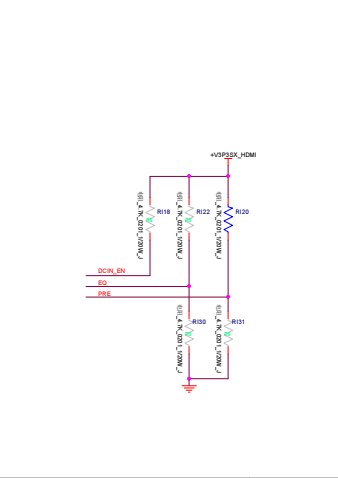
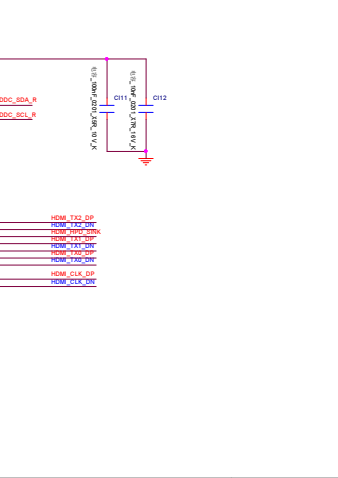
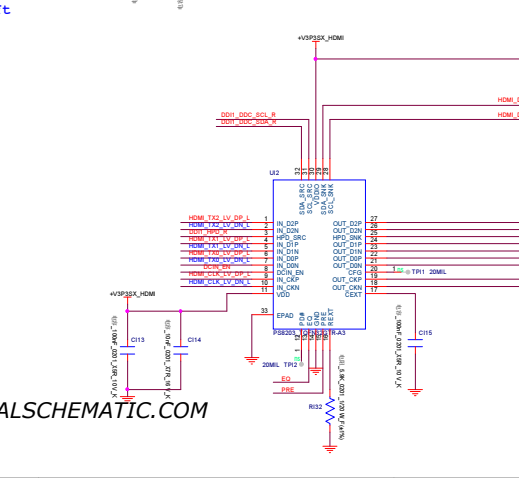
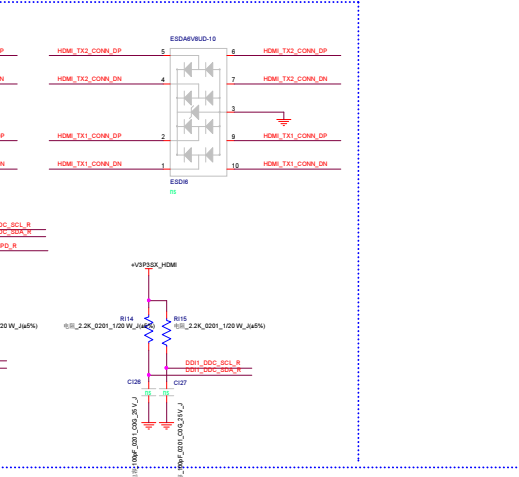
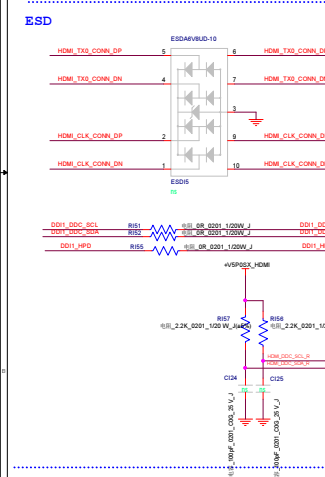
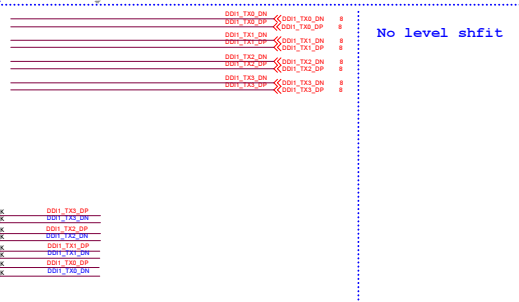
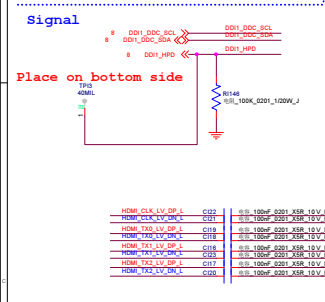
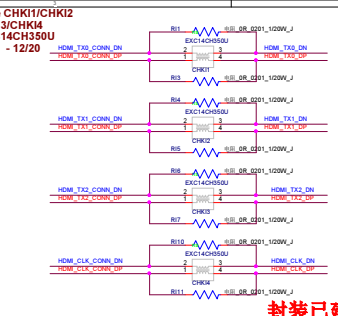
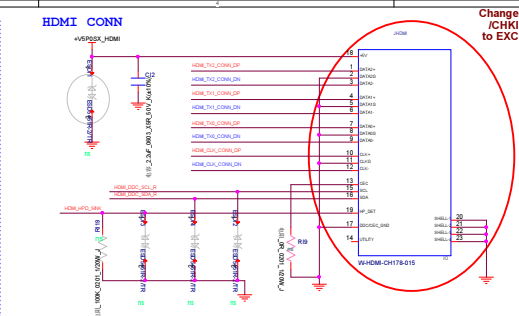
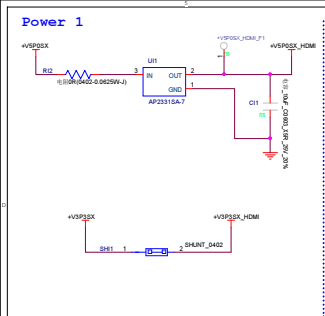






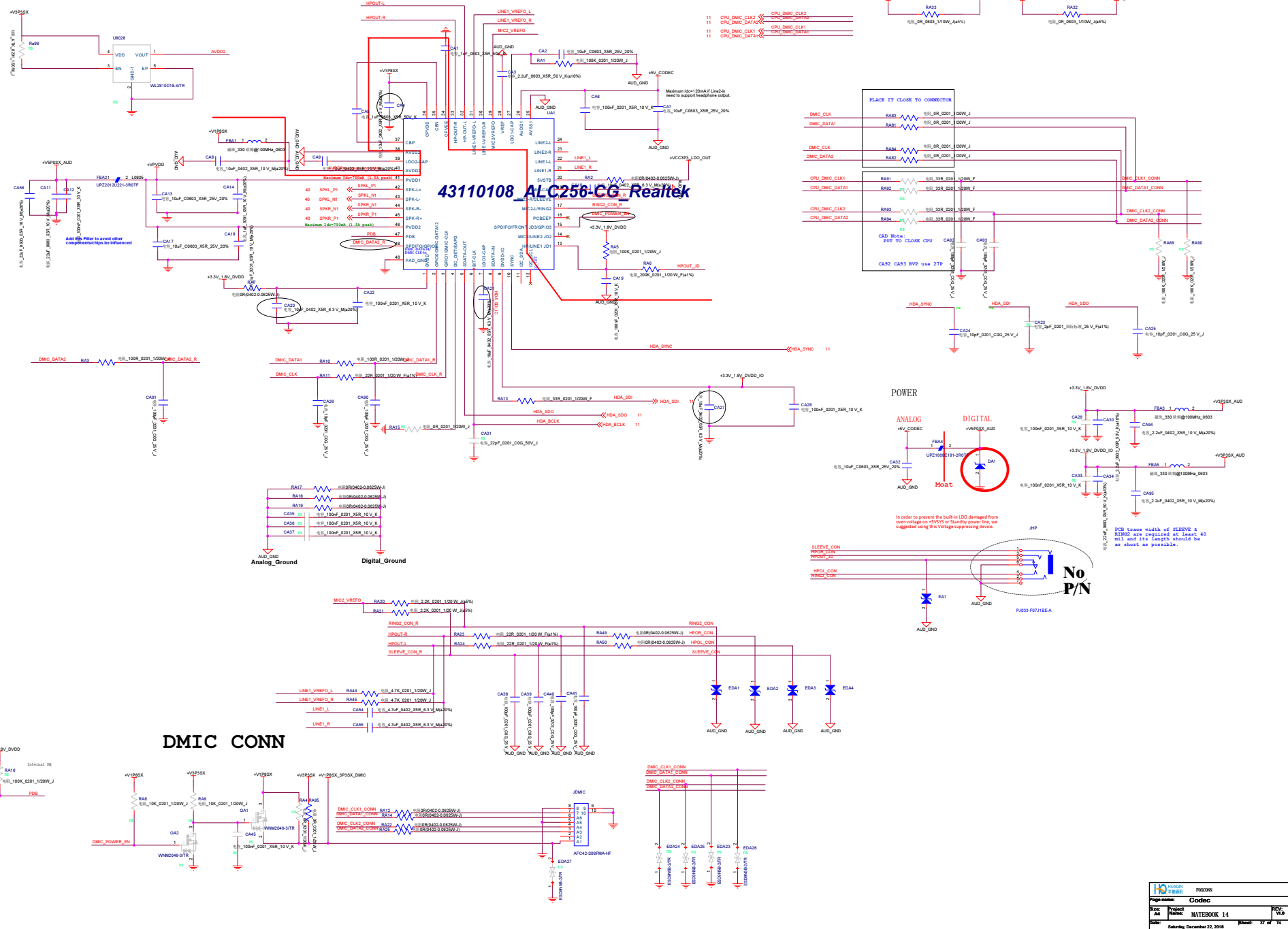
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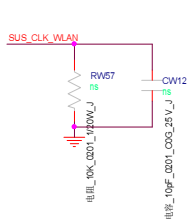
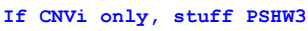
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Size: A4	Project Name:	MATEBOOK 14	REV: V1.0
Date:	Saturday, December 15, 2018		Sheet: 34 of 74



[HTTPS://REALSCHEMATIC.COM](https://realschematic.com)

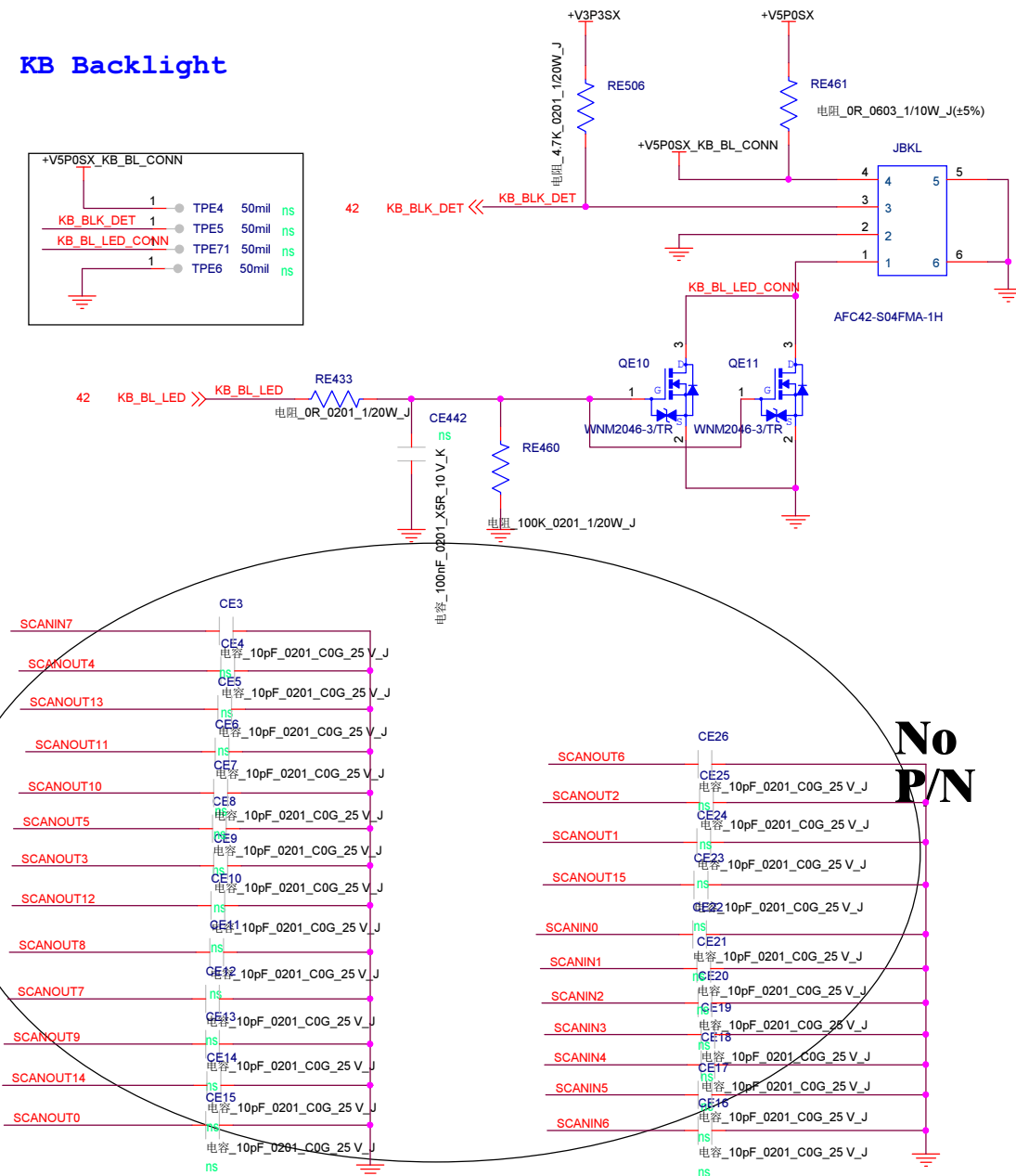
Power requirement:-		
DVDD must >=DVDD_IO.		
+3.3V_1.8V DVDD	+3.3V_1.8V DVDD IO	Result:
3.3V+/-10%	3.3V+/-10%	support:
3.3V+/-10%	1.8V+/-5%	support:
1.8V+/-5%	1.8V+/-5%	support:
1.8V+/-5%	1.5V+/-5%	support:
1.8V+/-5%	3.3V+/-10%	Not support:



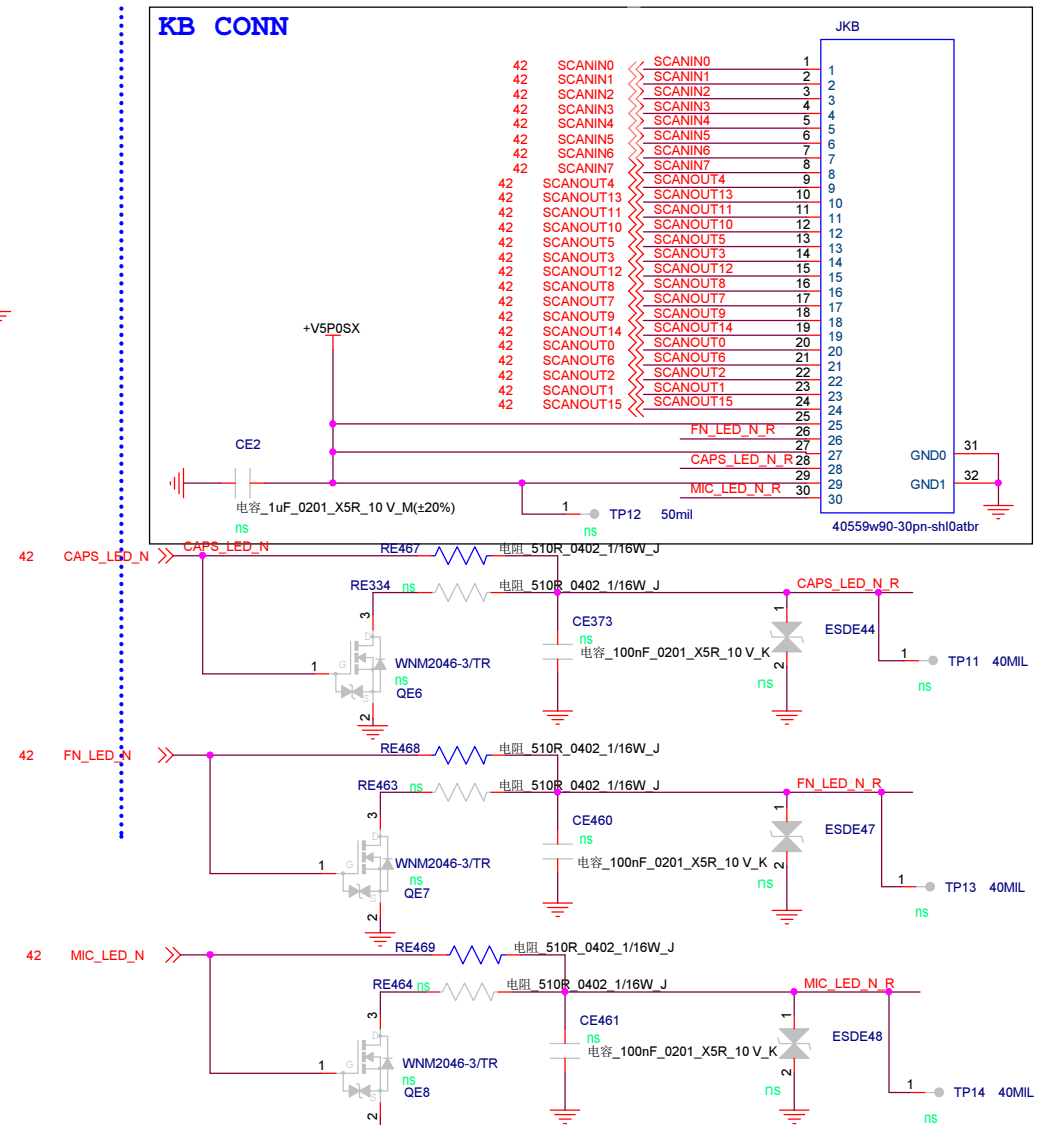


+V5POSX_KB_BL_CONN

Signal	Pin	Trace Width	Length
KB_BLK_DET	1	50mil	ns
KB_LED_CONN	1	50mil	ns
	1	50mil	ns
	1	50mil	ns

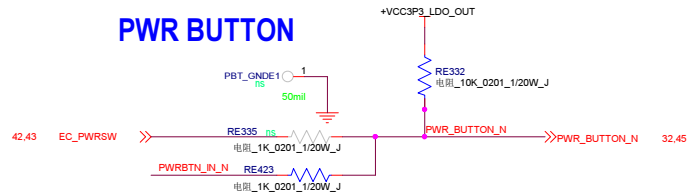


No P/N

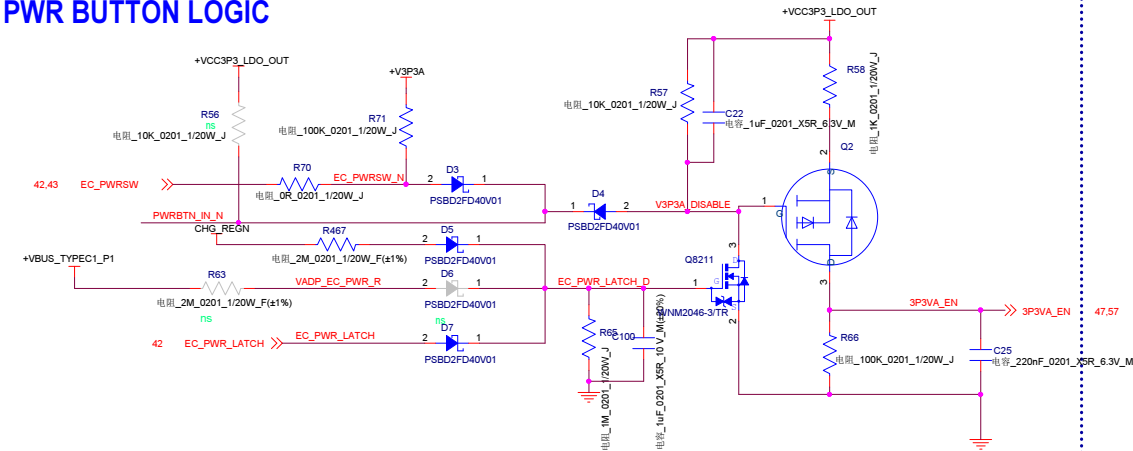




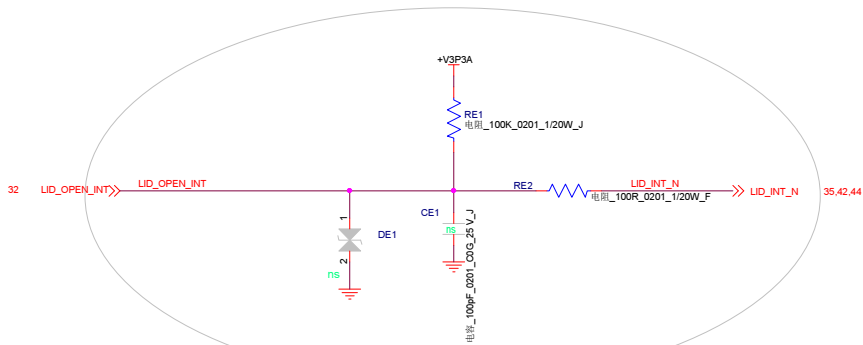
PWR BUTTON



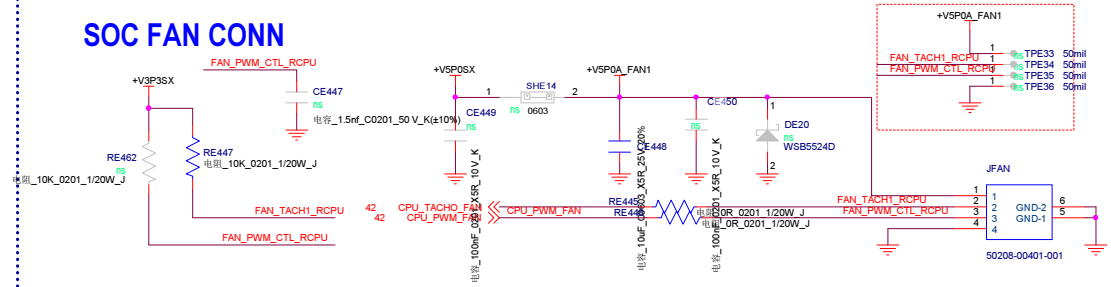
PWR BUTTON LOGIC



HALL

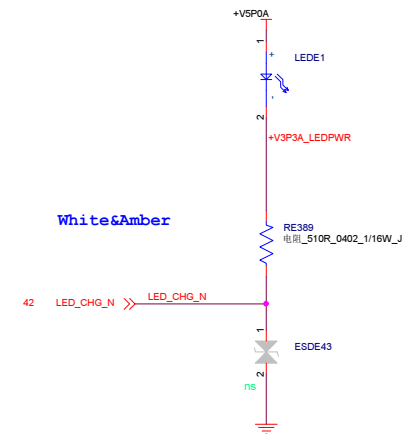



SOC FAN CONN



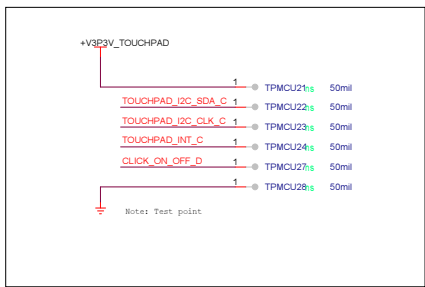
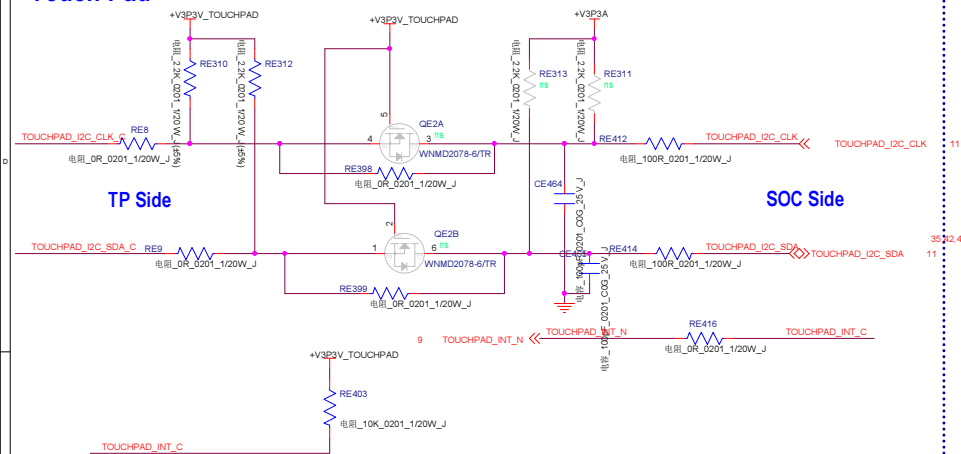
FOR product line

LED



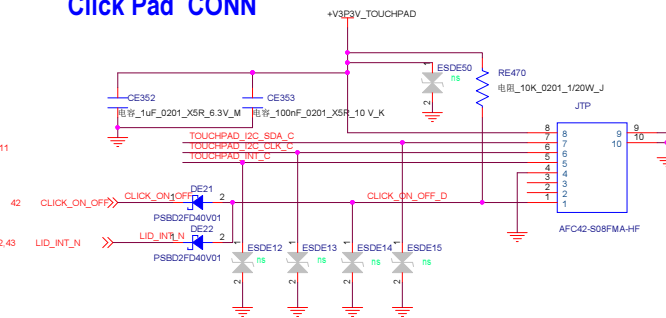
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Page name: BUTTON/FAN/LED/Hall			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 43 of 74		


Touch Pad

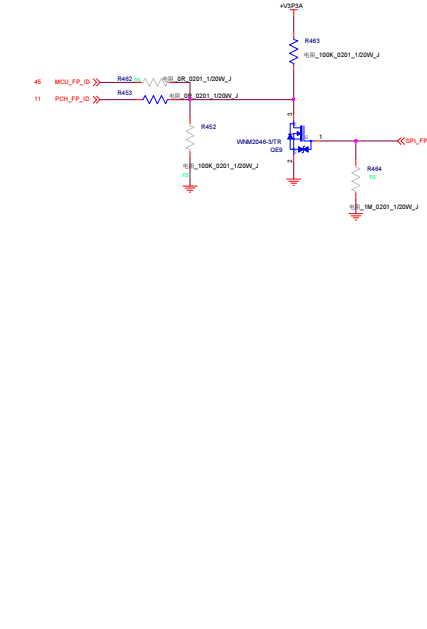
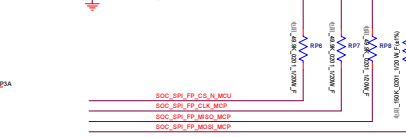
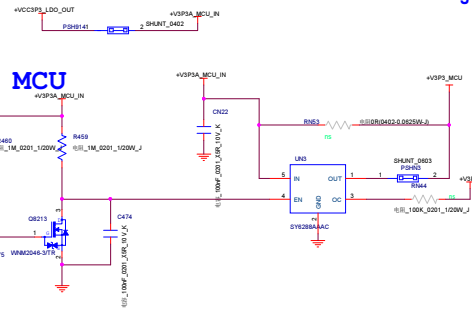


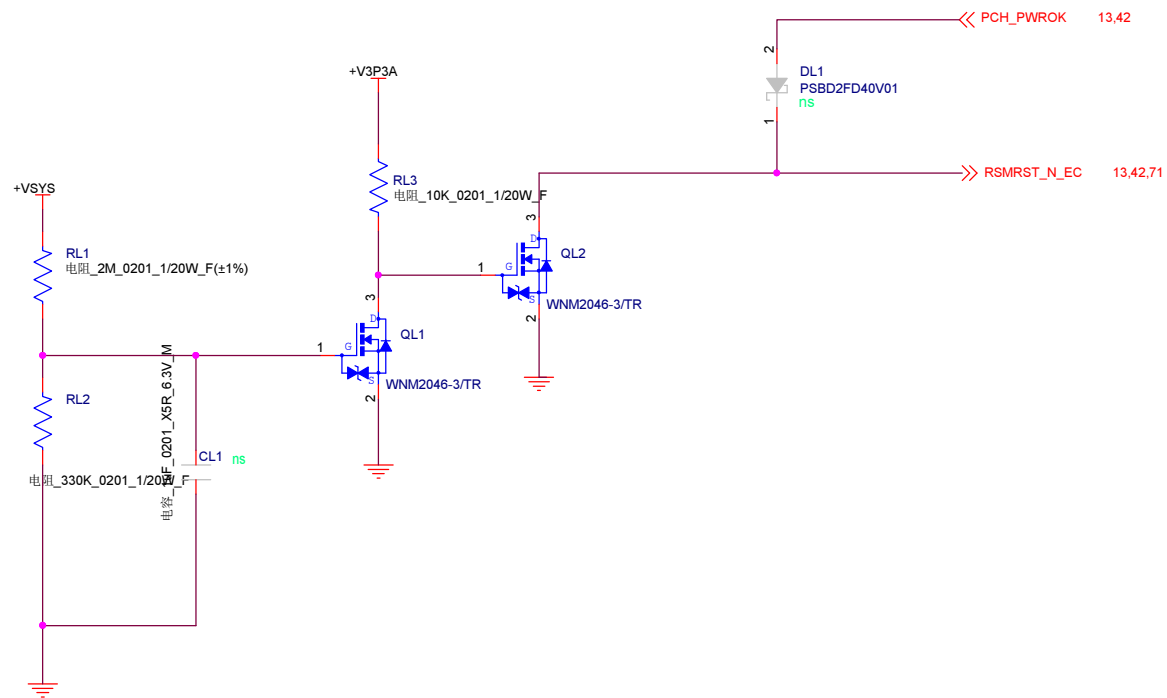
Click Pad CONN


PIN1对Pin1



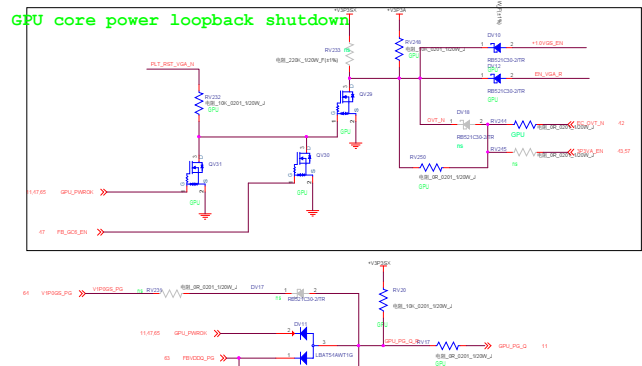
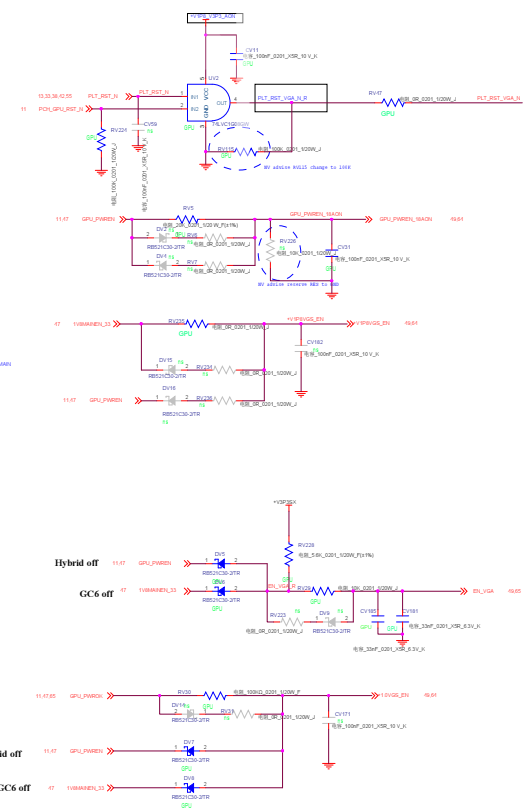
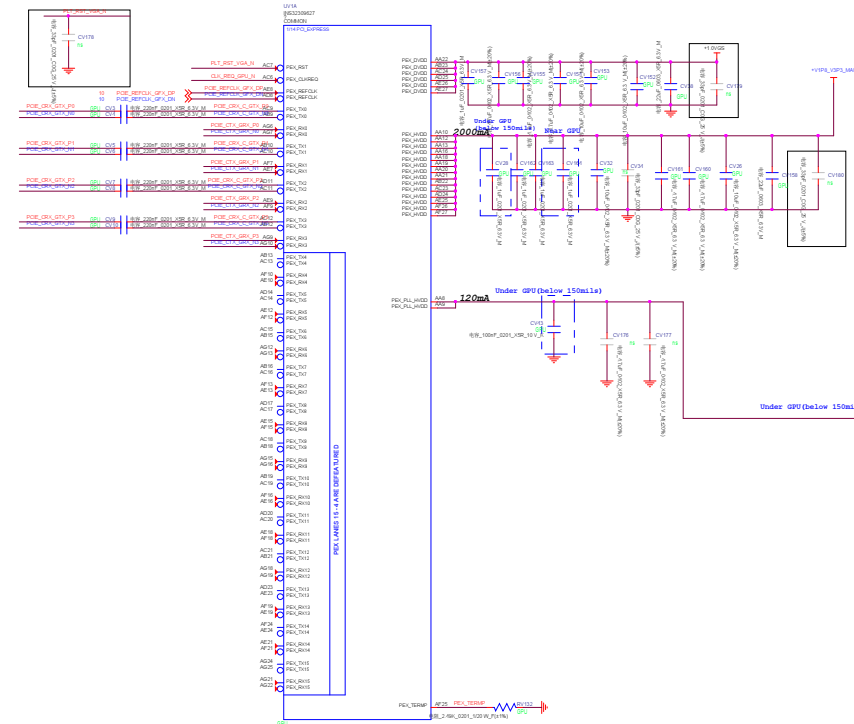
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Date: Saturday, December 15, 2018	Sheet: 44	of 74	

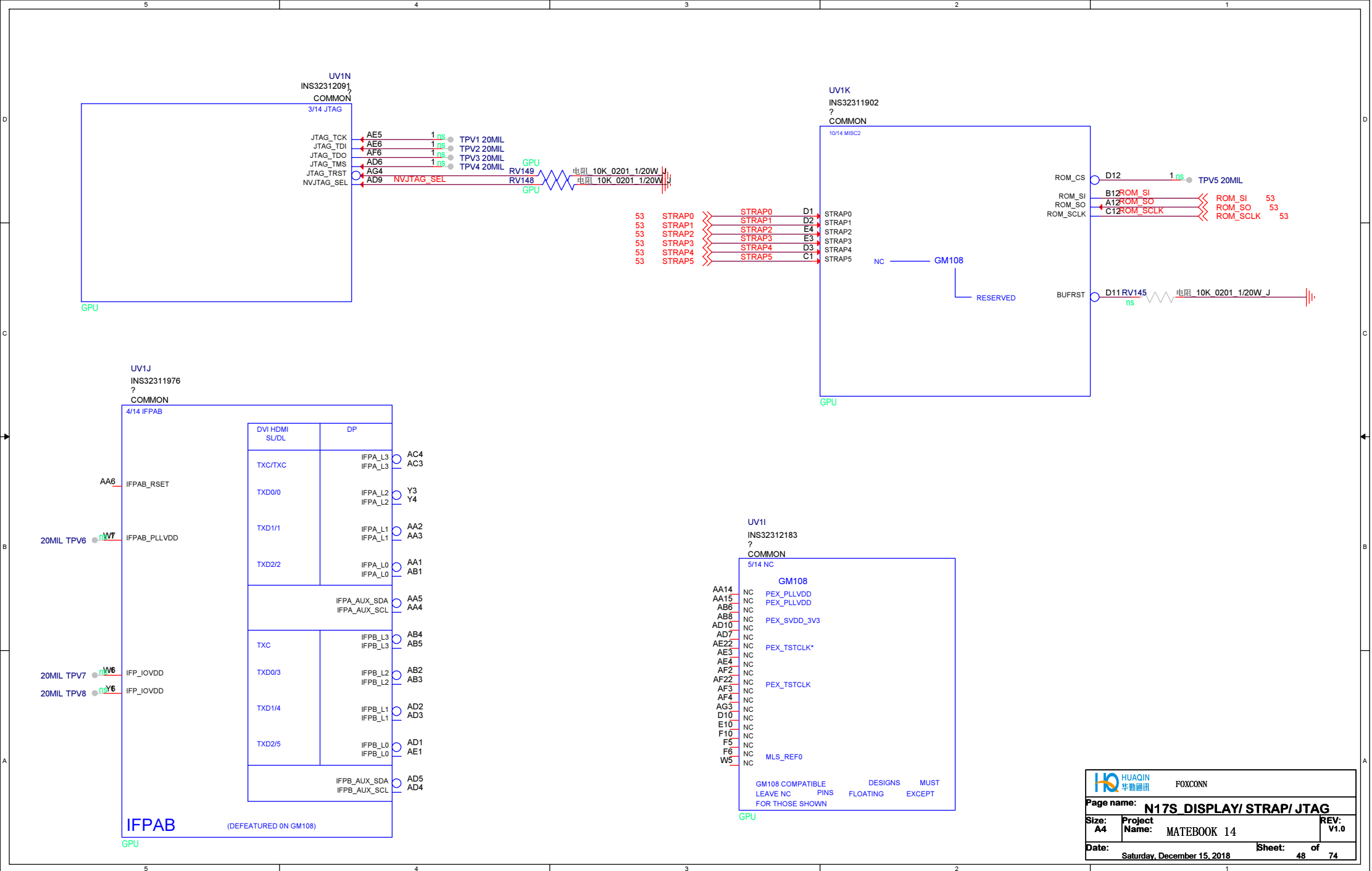
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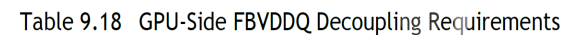


		FOXCONN	
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Date: Saturday, December 15, 2018	Sheet: 46	of 74	

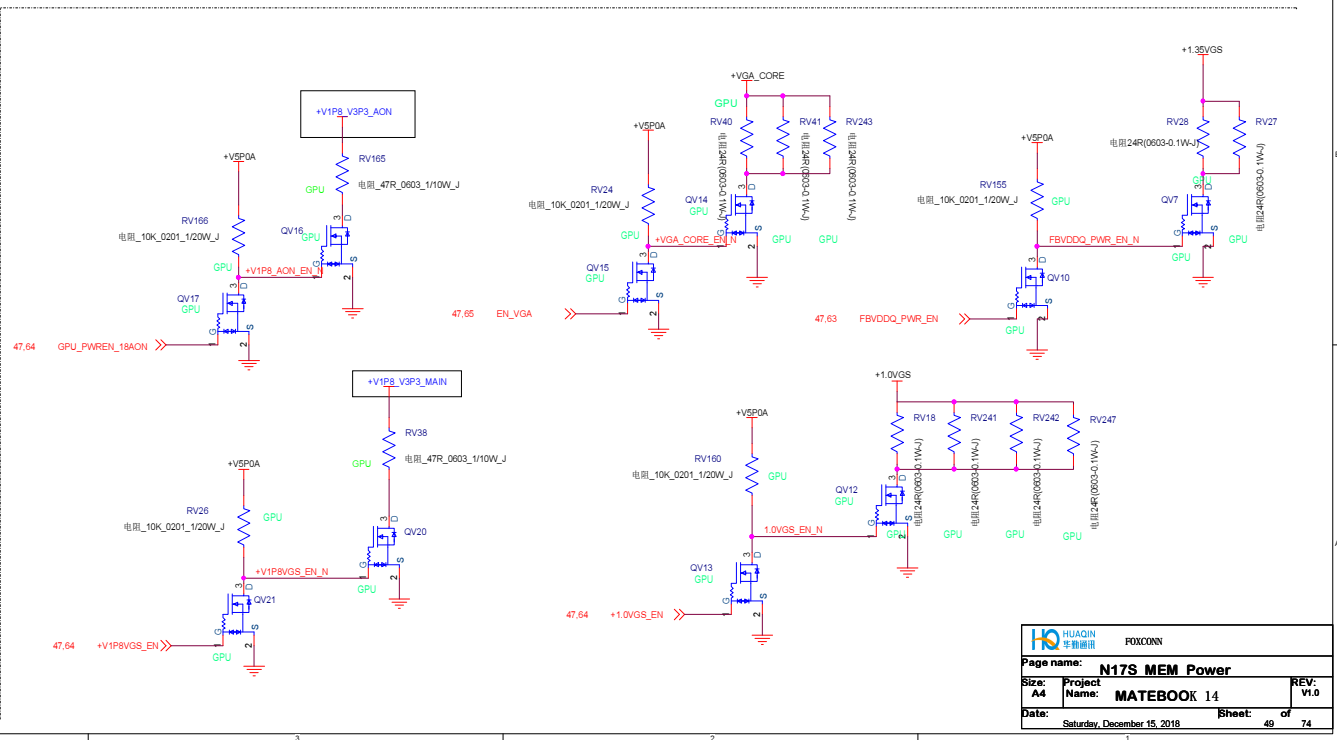
- 12 PDE_CSTX_CLK_0-3
- 12 PDE_CSTX_CLK_0-3
- 12 PDE_CSTX_CLK_0-3
- 12 PDE_CSTX_CLK_0-3

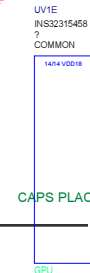
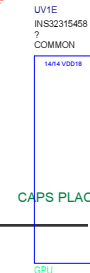
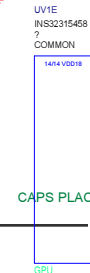






FBVDDQ Decoupling Requirements		
	Recommended Quantity and Placement (for all supported partitions combined)	
Size	Quantity	Placement
2C-64 (preliminary)		
65 [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
65 [0603]	2	
65 [0603]	1	Near GPU device
65 [0603]	3	
4C-128 (preliminary)		
65 [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
65 [0603]	4	
65 [0603]	2	Near GPU device
65 [0603]	5	
B4-256		
65 [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
65 [0603]	5	
65 [0603]	7	Near GPU device
65 [0603]	9	



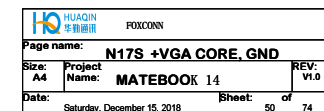


Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 1X 2.2uF (0603) 2 X 4.7uF (0603) Away from GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	Near GPU: 1X 2.2uF (0603) 2 X 4.7uF (0603) Away from GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 1X 2.2uF (0603) 2 X 4.7uF (0603) Away from GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1X 1uF (0402) 1X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1X 1uF (0402) 1 X 4.7uF (0603)

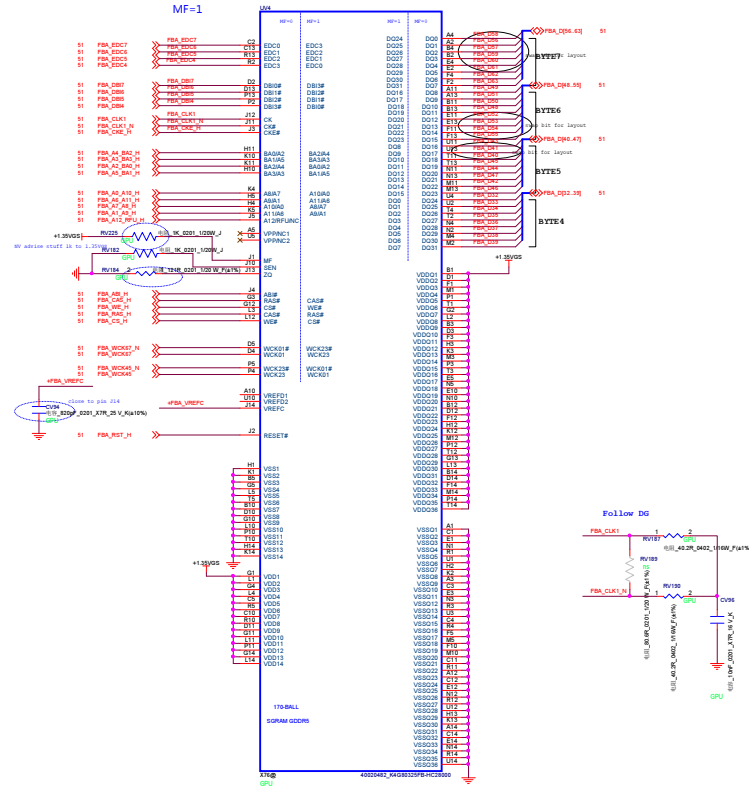
Note: 1. All capacitors are ceramic capacitors unless otherwise specified.
2. All capacitors are 20% tolerance unless otherwise specified.
3. All capacitors are 105°C rated unless otherwise specified.
4. All capacitors are 0.1% tolerance unless otherwise specified.
5. All capacitors are 0.1% tolerance unless otherwise specified.

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 1X 2.2uF (0603) 2 X 4.7uF (0603) Away from GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	Near GPU: 1X 2.2uF (0603) 2 X 4.7uF (0603) Away from GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 1X 2.2uF (0603) 2 X 4.7uF (0603) Away from GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1X 1uF (0402) 1X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1X 1uF (0402) 1 X 4.7uF (0603)

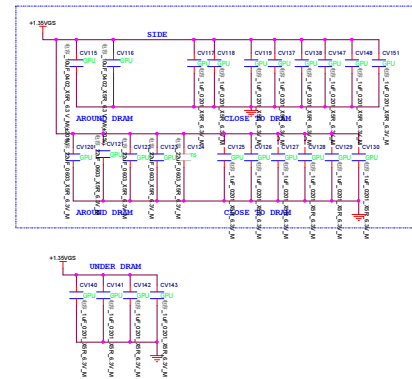
Note: 1. All capacitors are ceramic capacitors unless otherwise specified.
2. All capacitors are 20% tolerance unless otherwise specified.
3. All capacitors are 105°C rated unless otherwise specified.
4. All capacitors are 0.1% tolerance unless otherwise specified.
5. All capacitors are 0.1% tolerance unless otherwise specified.

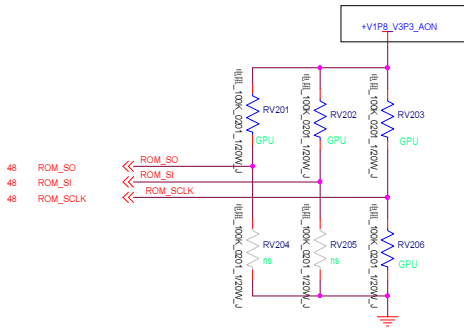
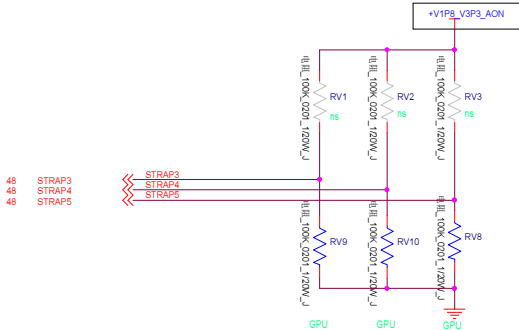
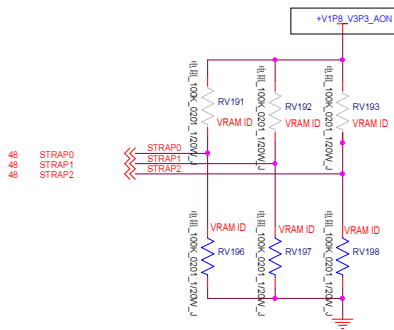


Memory - Upper 32 bits



Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM Interface Mode)
Combined FBVDD-FBVDDQ Rail			
1.0 uF	X6S [4062]	10	For x32 DRAM: Under the DRAM FBVDD or FBVDDQ ball. For x16 DRAM in a "clashless" PCB configuration: As close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.
10 uF	X6S [6603]	4	
1.0 uF	X6S [4062]	8 additional	For x32 DRAM: Choose x32 interface to allow high speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible. See Figure 9-23 for an example.
10 uF	X6S [6603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X6S [6603]	5	For 4 Gb/s WCK (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.





HQ PN	MPN	Strap	Vendor
HQ11121763000	H5GC8H24AJR-R2C	0xA	Hynix
HQ11121761000	MT51J256M32HF-80:B	0x9	Micron

Table 5. N175-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A

Notes:

- For N175-G0/G2, the maximum allowable memory case temperature is 85 °C.
- N175-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations

SMBUS_ALT_ADDR	DEVID_SEL
0 0x9E (Default)	0 (Default)
1 0x9C (Multi-GPU usage)	1

PCIE_CFG	VGA_DEVICE
0 (Default)	0 3D Device (Class Code 302h)
1	1 VGA Device (Default)

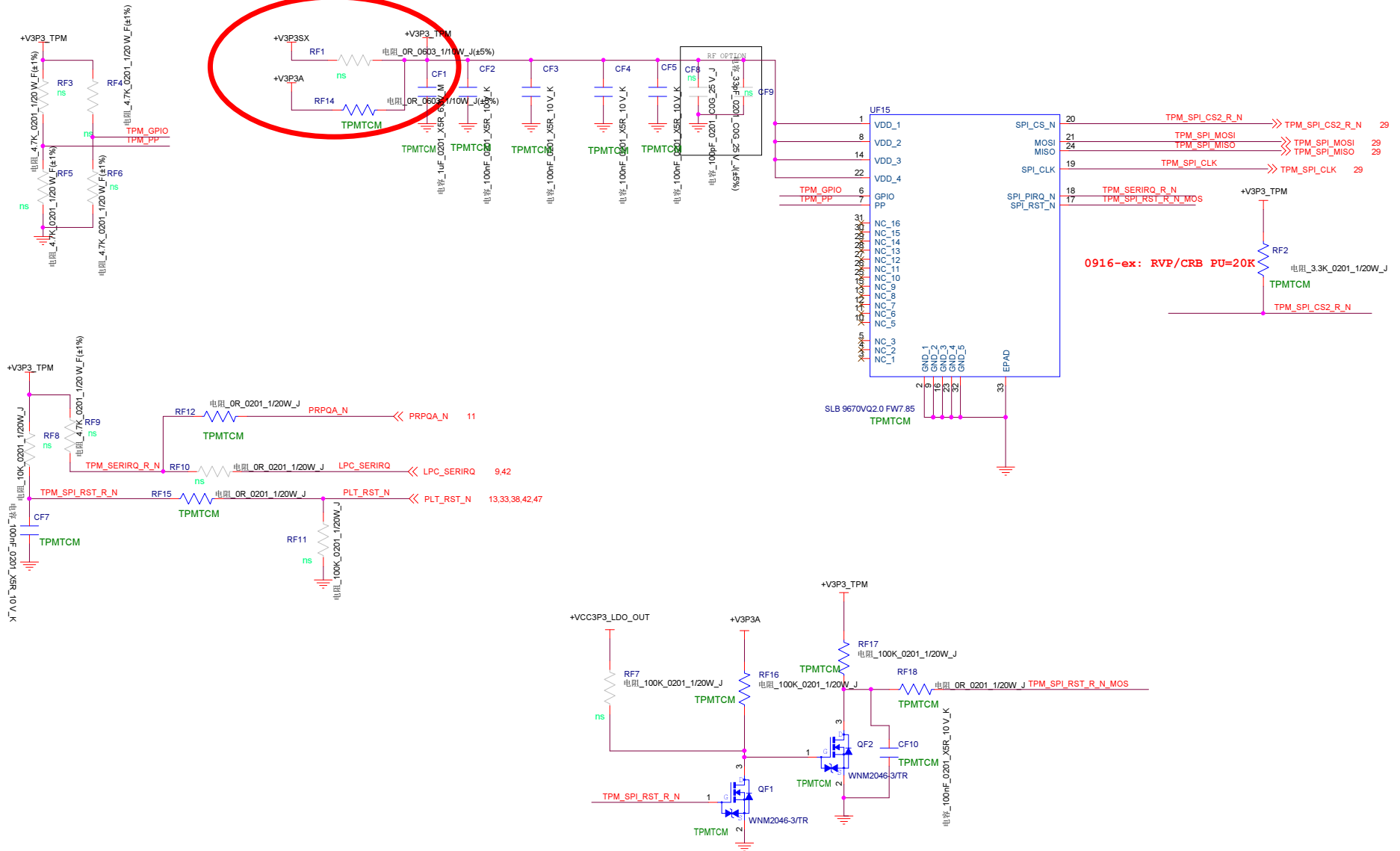
Table 5.3 RAMCFG

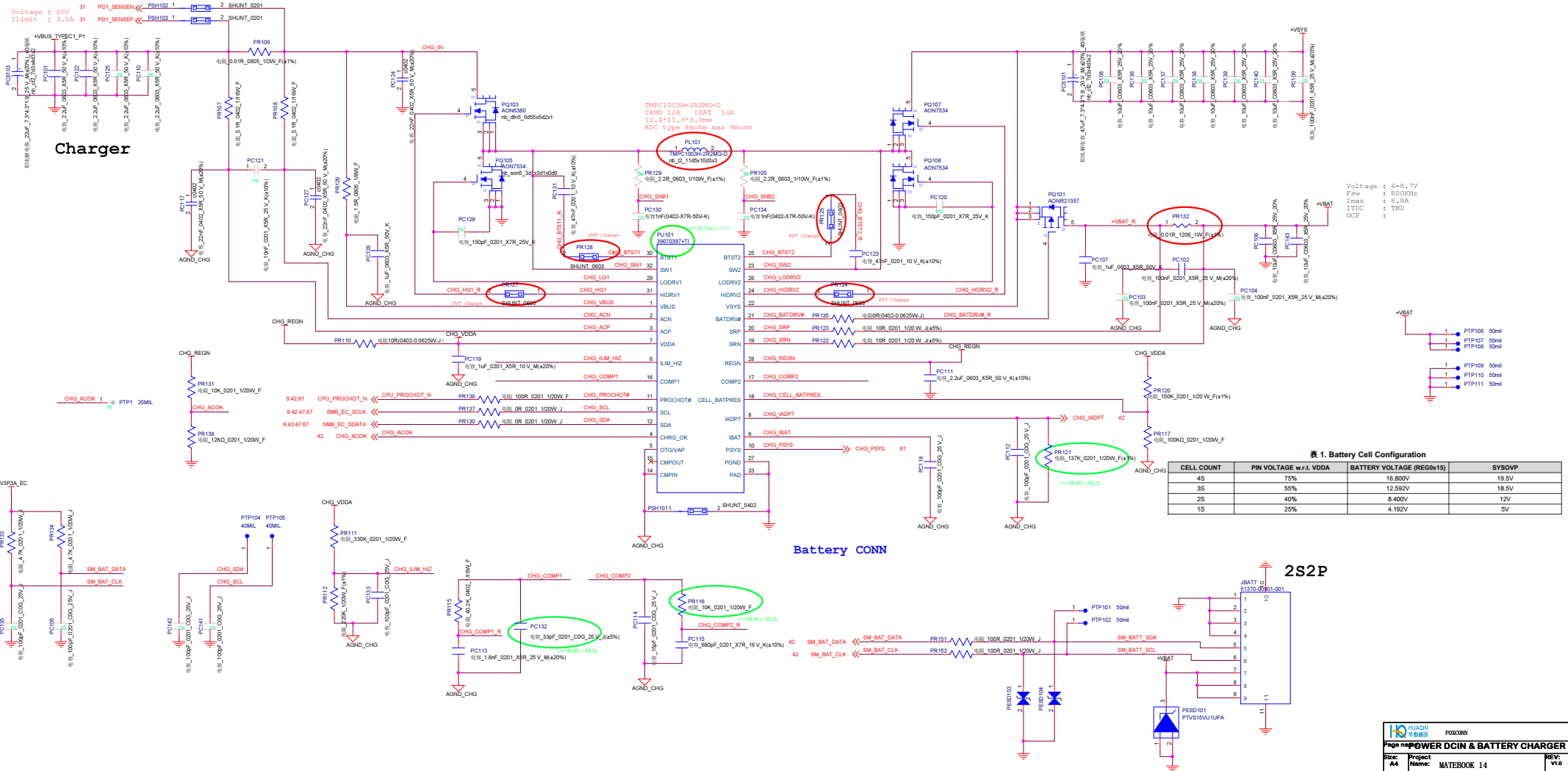
Strap Pins <small>see Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Physical Strapping pin	Power Rail	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SCLK	M				
ROM_SI	H	Disable	Disable	Disable	Disable
ROM_SO	H				

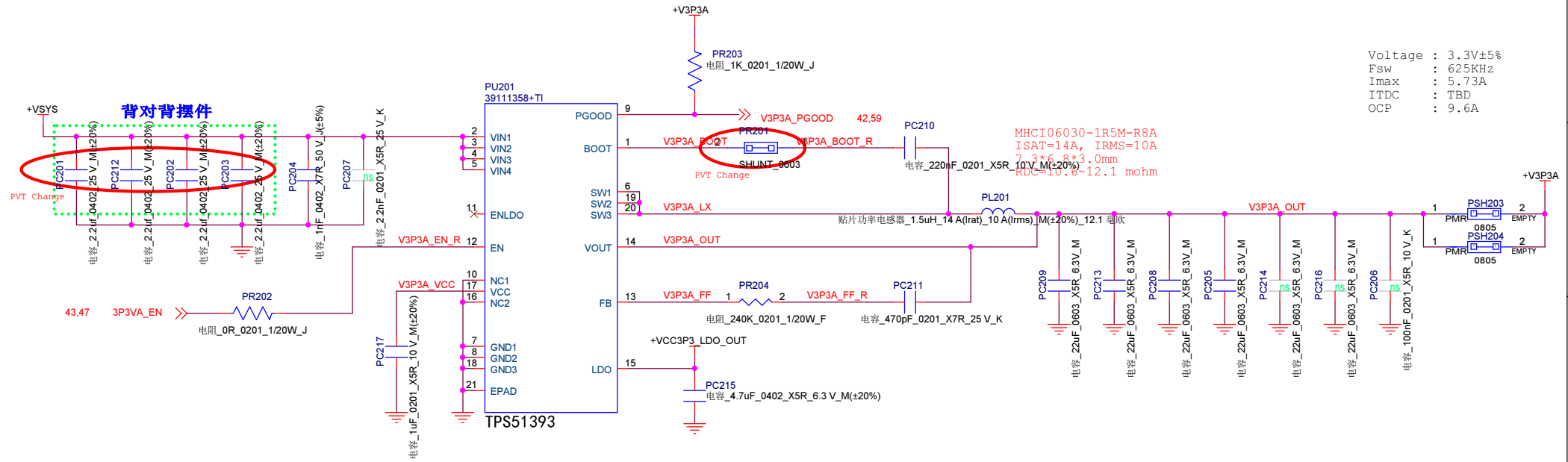



to check the PWR well
for TPM/TCM to avoid
leakage, to +V3P3A?

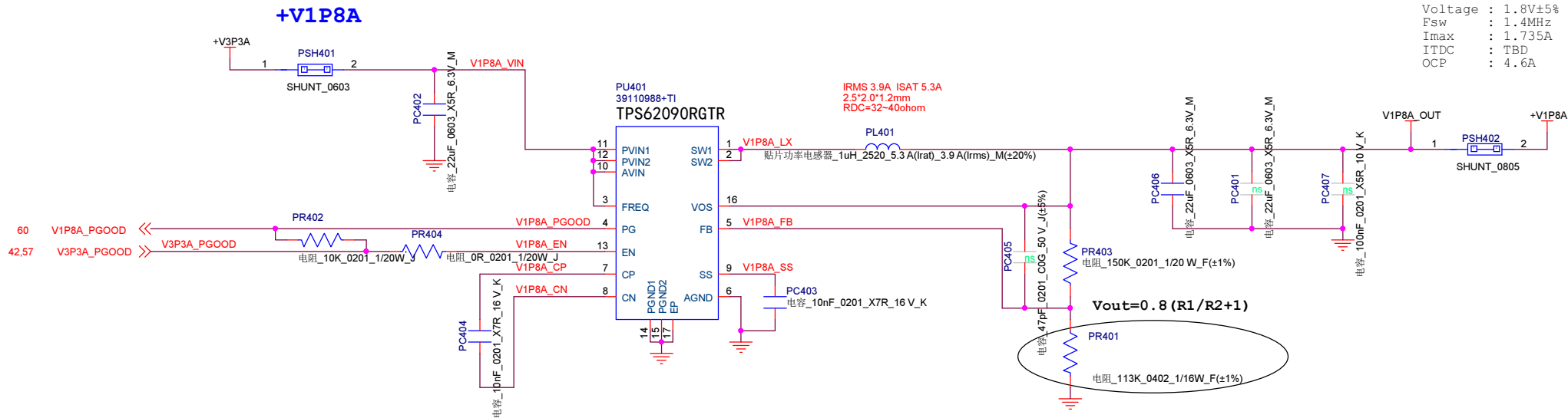





+V3P3A



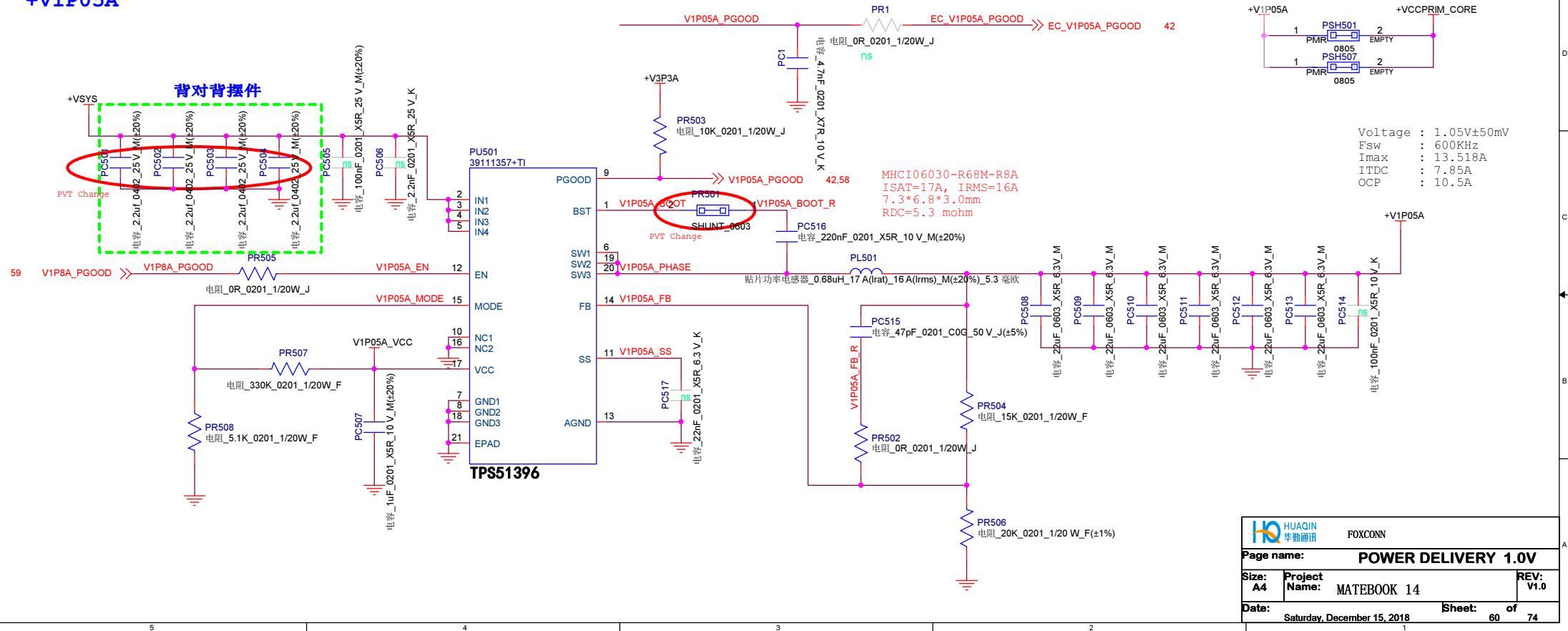
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Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 57	of 74	




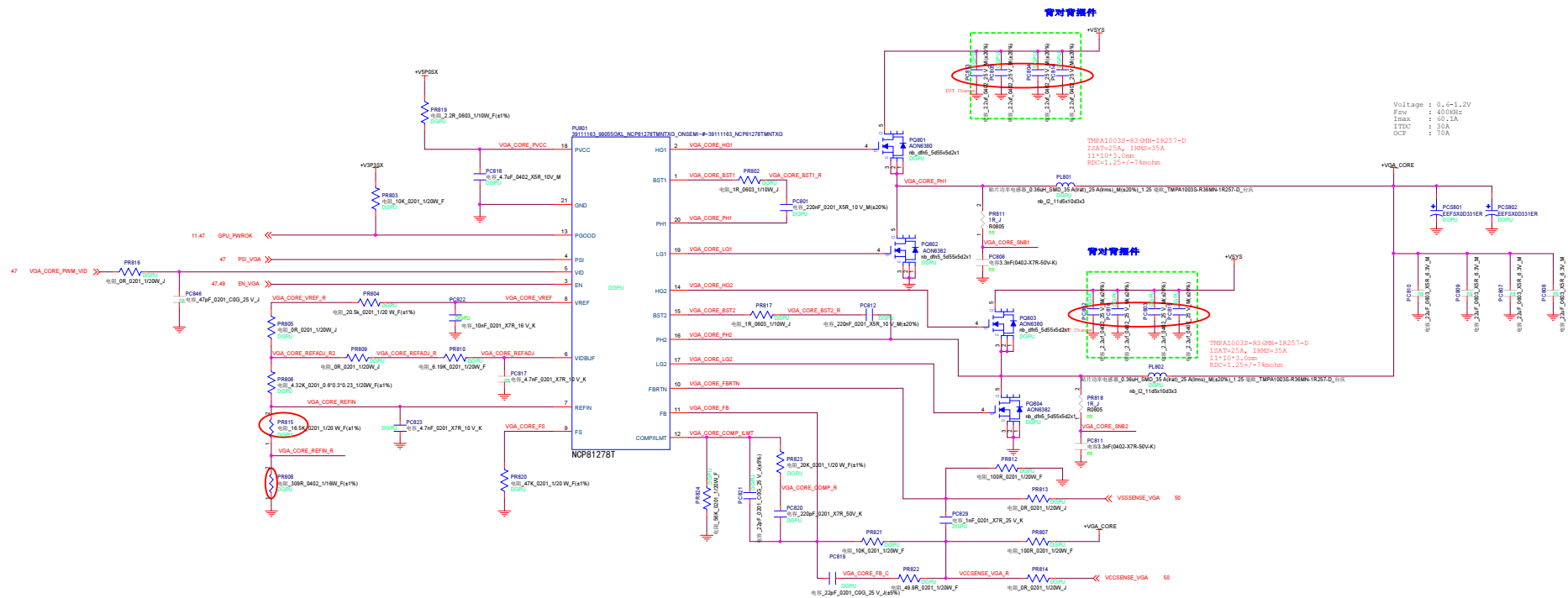
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Date: Saturday, December 15, 2018	Sheet: 59	of 74	

+V1P05A

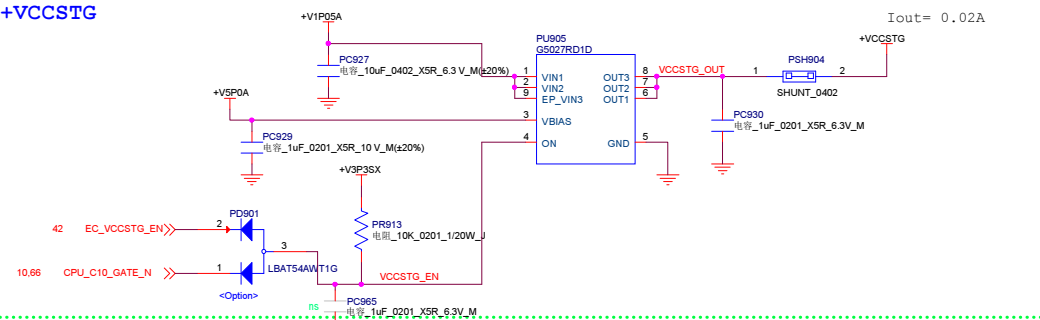
背对背摆件



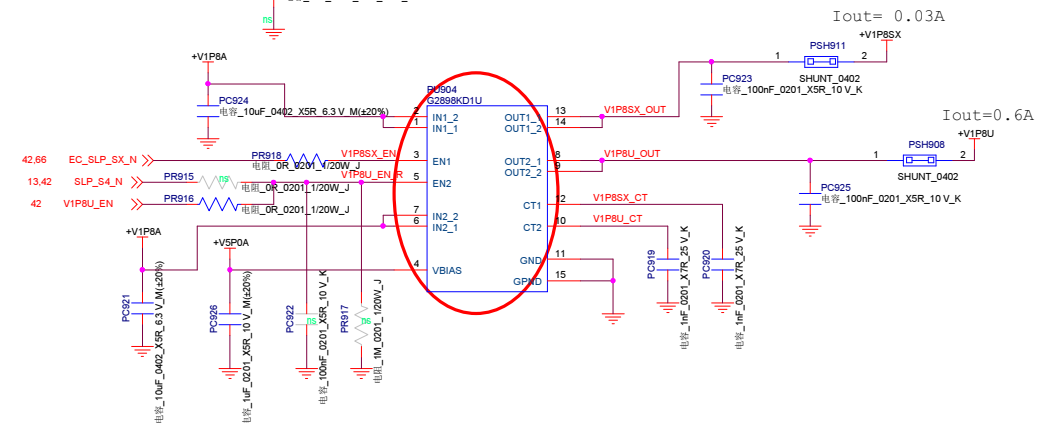
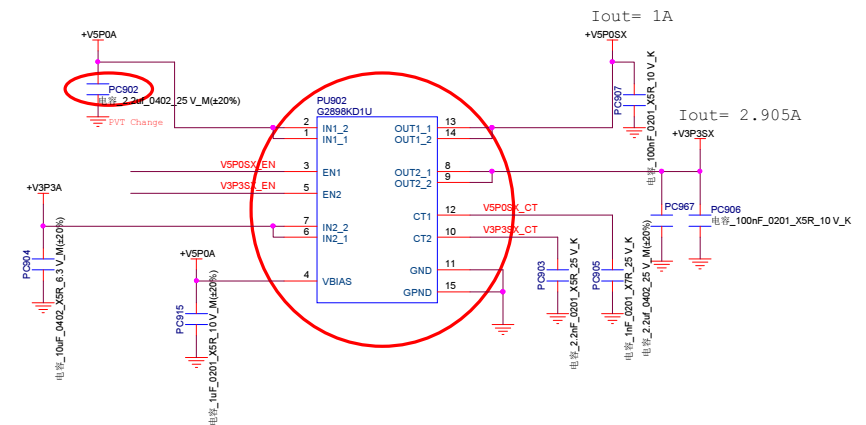
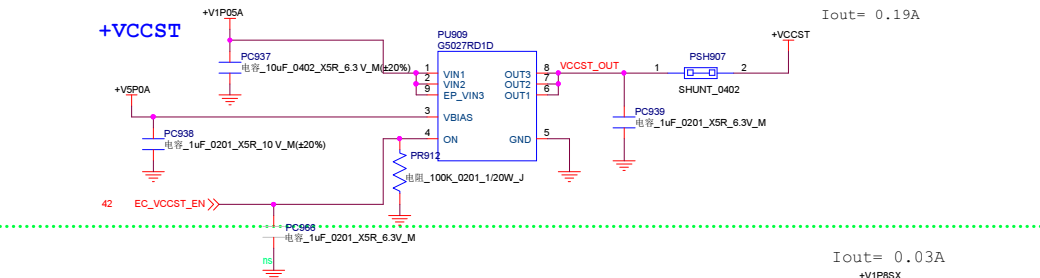
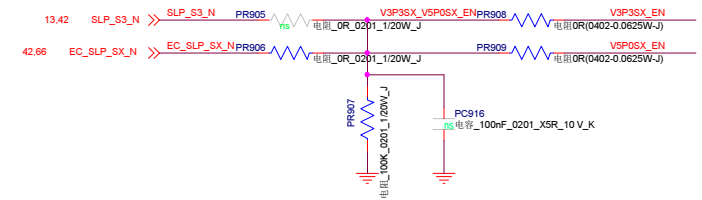
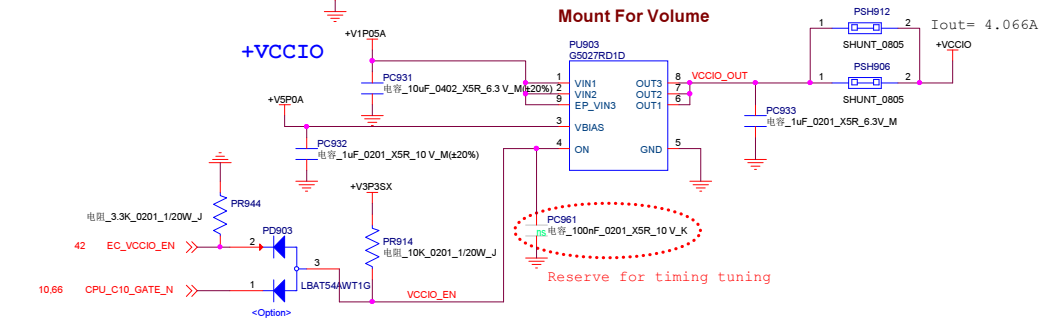
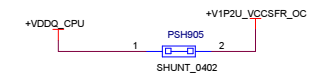
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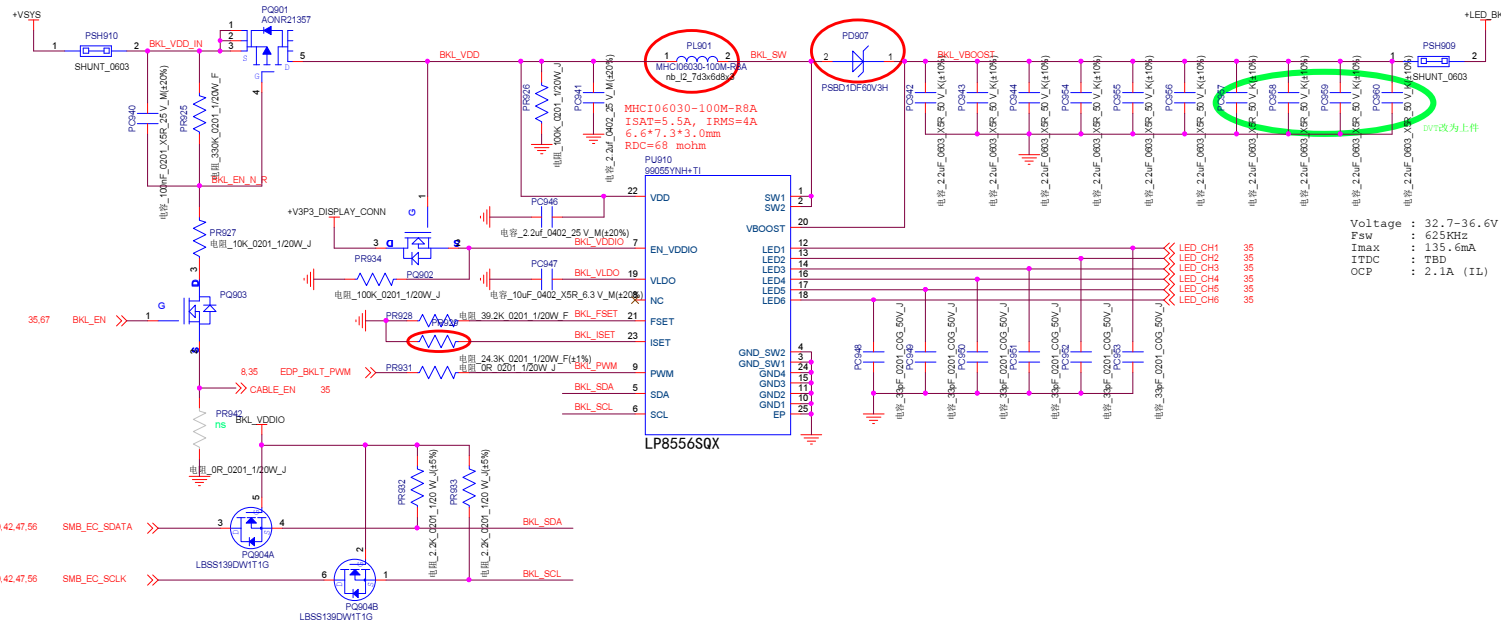
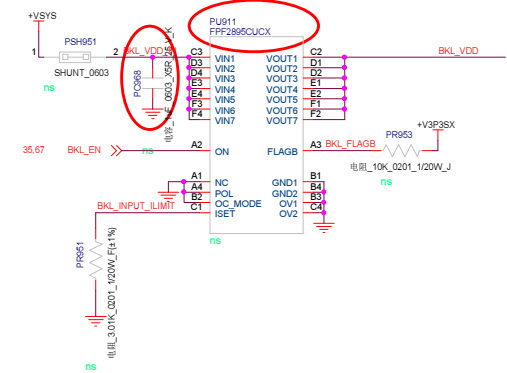


+VCCSTG

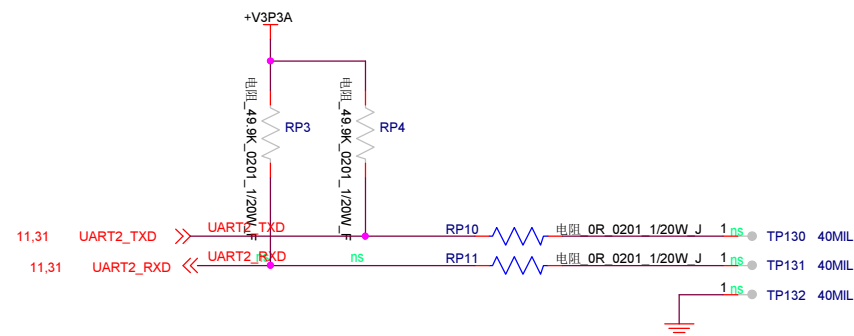
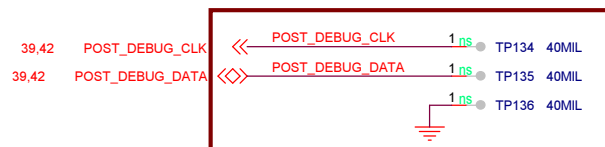
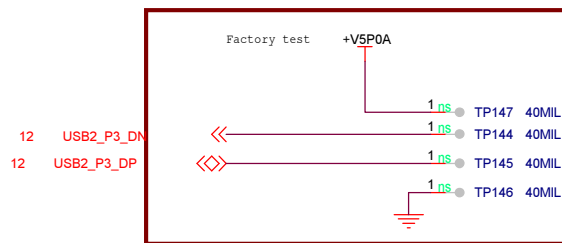



+V1P2U VCCSFR OC

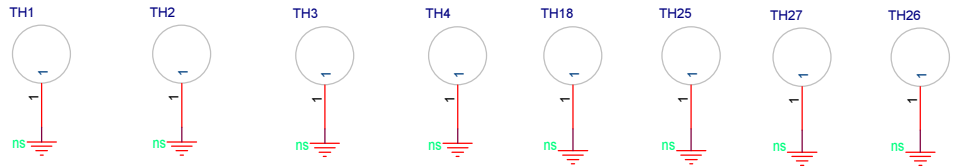




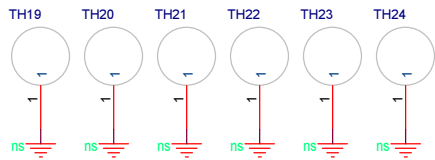
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 Fsw : 625KHz
 Imax : 135.6mA
 ITDC : TBD
 OCP : 2.1A (IL)



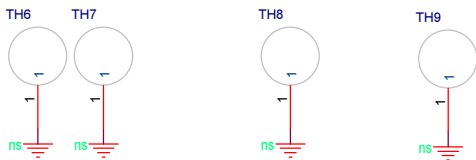
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Date: Saturday, December 15, 2018	Sheet: 68	of 74	



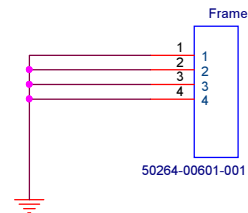
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nb_pthc3hc6 数量: 1
nb_pthc1d9hc4d5 数量: 1
nb_pthc1d9hc4 数量: 1
nb_pthc1d9hc3d5 数量: 1
nb_pthc1d9hc4 数量: 1




nb_pth3d4hc4d4 数量: 6




nb_pthc3d2htc5d2bc6 数量: 2
nb_pthc2d8hc4d4 数量: 1
nb_pthc1d8htc5d5bc4d5 数量: 1



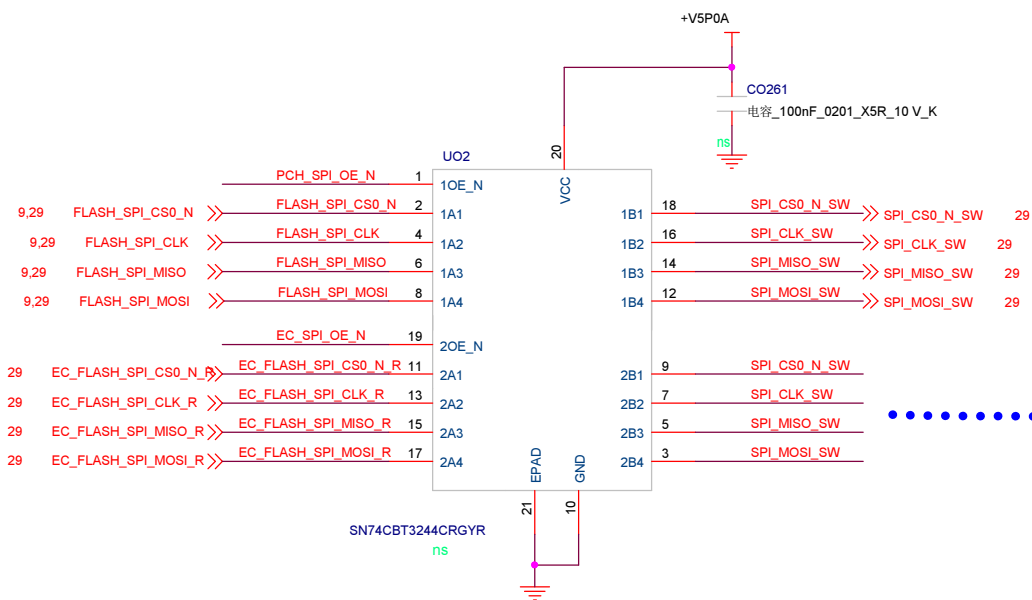
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Page name: Hole & Mark			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
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D					
C					
B					
A					

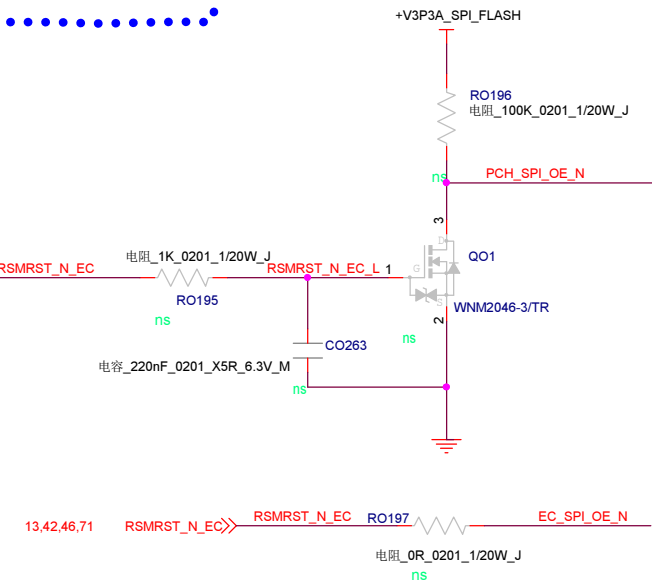
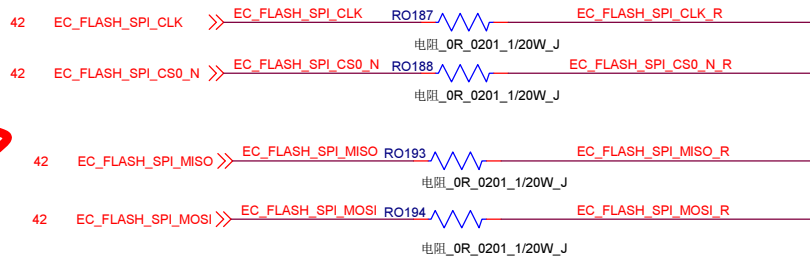
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Size: A4	Project Name: MATEBOOK 14		REV: V1.0
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Rvsd For PCH and EC SPI Isolation

0918-ex:
From PCH



0918-ex:
From EC



HUAQIN 华勤通信		FOXCONN	
Page name:		SPI MOSFET	
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